FLUKE®

Instruction Manual

NOTE

This manual documents the Model 7250A Universal Counter-Timer and its assemblies at the revision levels shown in Appendix 7A. If your instrument contains assemblies with different revision letters, it will be necessary for you to either update or backdate this manual. Refer to the supplemental change/errata sheet for newer assemblies, or to the backdataing sheet in Appendix 7A for older assemblies.

Model

7250A

Universal Counter-Timer

P/N 487496

December 1978

WARRANTY

Notwithstanding any provision of any agreement the following warranty is exclusive:

The JOHN FLUKE MFG. CO., INC., warrants each instrument it manufactures to be free from defects in material and workmanship under normal use and service for the period of 1-year from date of purchase. This warranty extends only to the original purchaser. This warranty shall not apply to fuses, disposable batteries (rechargeable type batteries are warranted for 90-days), or any product or parts which have been subject to misuse, neglect, accident or abnormal conditions of operations.

In the event of failure of a product covered by this warranty, John Fluke Mfg. Co., Inc., will repair and calibrate an instrument returned to an authorized Service Facility within 1 year of the original purchase; provided the warrantor's examination discloses to its satisfaction that the product was defective. The warrantor may, at its option, replace the product in lieu of repair. With regard to any instrument returned within one year of the original purchase, said repairs or replacement will be made without charge. If the failure has been caused by misuse, neglect, accident or abnormal conditions of operations, repairs will be billed at a nominal cost. In such case, an estimate will be submitted before work is started, if requested.

THE FOREGOING WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTY OF MERCHANTABILITY, FITNESS OR ADEQUACY FOR ANY PARTICULAR PURPOSE OR USE. JOHN FLUKE MFG. CO., INC., SHALL NOT BE LIABLE FOR ANY SPECIAL, INCIDENTAL OR CONSEQUENTIAL DAMAGES, WHETHER IN CONTRACT, TORT OR OTHERWISE.

If any failure occurs, the following steps should be taken:

1. Notify the JOHN FLUKE MFG. CO., INC., or the nearest Service facility, giving full details of the difficulty, and include the Model number, type number, and serial number. On receipt of this information, service data or shipping instructions will be forwarded to you.

2. On receipt of the shipping instructions, forward the instrument, transportation prepaid. Repairs will be made at the Service Facility and the instrument returned, transportation prepaid.

SHIPPING TO MANUFACTURER FOR REPAIR OR ADJUSTMENT

All shipments of JOHN FLUKE MFG. CO., INC., instruments should be made via United Parcel Service or "Best Way" prepaid. The instrument should be shipped in the original packing carton; or if it is not available, use any suitable container that is rigid and of adequate size. If a substitute container is used, the instrument should be wrapped in paper and surrounded with at least four inches of excelsior or similar shock-absorbing material.

CLAIM FOR DAMAGE IN SHIPMENT TO ORIGINAL PURCHASER

The instrument should be thoroughly inspected immediately upon original delivery to purchaser. All material in the container should be checked against the enclosed packing list. The manufacturer will not be responsible for shortages against the packing sheet unless notified immediately. If the instrument is damaged in any way, a claim should be filed with the carrier immediately. (To obtain a quotation to repair shipment damage, contact the nearest Fluke Technical Center.) Final claim and negotiations with the carrier must be completed by the customer.

The JOHN FLUKE MFG. CO., INC. will be happy to answer all application or use questions, which will enhance your use of this instrument. Please address your requests or correspondence to: JOHN FLUKE MFG. CO., INC., P.O. BOX 43210, MOUNTLAKE TERRACE, WASHINGTON 98043, ATTEN: Sales Dept. For European Customers: Fluke (Nederland) B.V., Zevenheuvelenweg 53, Tilburg, The Netherlands.

* For European customers, Air Freight prepaid.

John Fluke Mfg. Co., Inc., • P.O. Box 43210 • Mountlake Terrace, Washington 98043

Rev. 9/78

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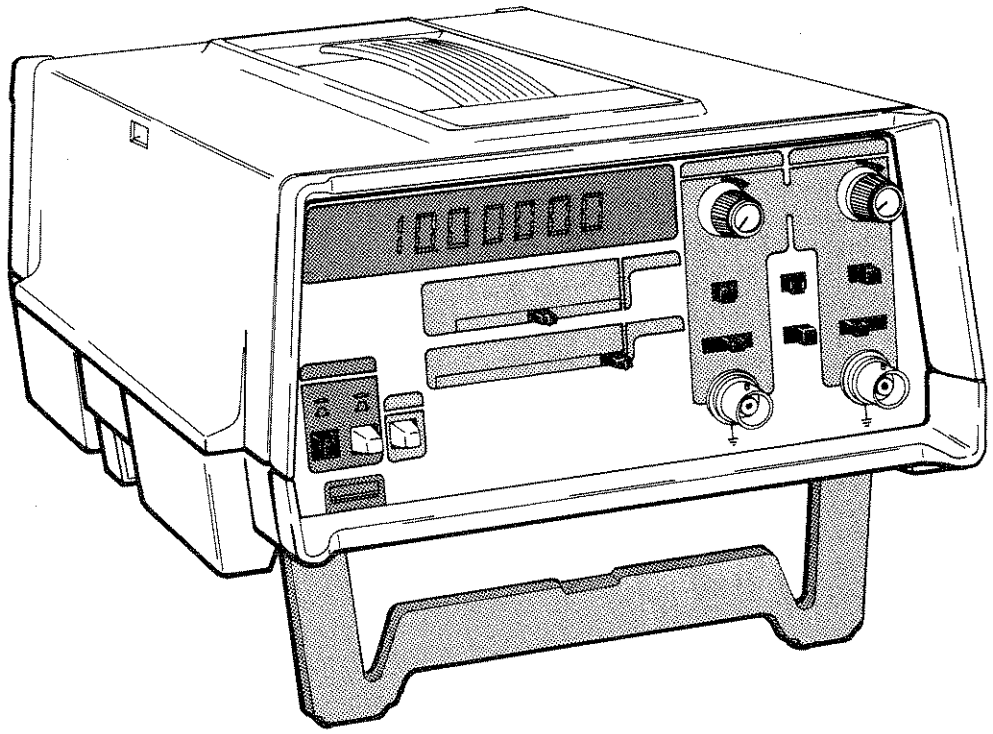


7250A Universal Counter-Timer

Section 1
Introduction & Specifications

1-1. INTRODUCTION

1-2. The Model 7250A is a Universal Counter-Timer capable of measurements in seven modes of operation: frequency (Channel A, 5 Hz to 80 MHz), period and period averaging (Channel A, 5 Hz to 1 MHz), time interval (Channel A to Channel B, 5 Hz to 2 MHz), counts per minute (Channel A, 5 Hz to 80 MHz), ratio of Channel A (5 Hz to 80 MHz) divided by Channel B (5 Hz to 1 MHz), and totalize Channel A (5 Hz to 80 MHz). In addition, Self Check mode is provided to demonstrate operability of most 7250A circuits.

1-3. This manual documents the 7250A Universal Counter-Timer under two categories. The standard instrument without options and accessories is covered in Sections 1 through 5, 7 and 8. All optional or accessory items are documented in Section 6; refer to Table 1-1 and 1-2 for a listing of available options and accessories. Schematic diagrams for the standard instrument and the options are centralized in Section 8.

1-4. DESCRIPTION

1-5. The Model 7250A is a seven-digit universal counter-timer capable of measurements in frequency, period, period average, time interval, totalize, ratio, and self check mode. In addition, counts per minute mode offers a direct readout of RPM when the instrument is attached to an appropriate transducer. The 7250A features six manually selected resolution settings, autoranging, leading zero suppression, full annunciation, autoreset, and a free-air crystal time base.

1-6. Each of the two 1 MΩ input channels is controlled by a ± slope control and a three position trigger level offset switch. Separate attenuation controls (continuously variable from X1 to X100) are provided for each input. A 100 kHz low pass filter can be applied to both channels. Channel A can be measured in common with, or separately from, Channel B. Input frequencies on Channel A can range from 5 Hz to 80 MHz. Channel B, when used in ratio and time interval measurements, has a maximum input of 2 MHz.

1-7. A number of options and accessories are available with the instrument. Improved time base stability can be realized with the optional TCXO, or with one of the oven time bases. Complete lists of options and accessories are presented in Tables 1-1 and 1-2.

1-8. SPECIFICATIONS

1-9. Specifications for the 7250A Universal Counter-Timer are listed in Table 1-3.

Table 1-1. 7250A Options

OPTION NO.	DESCRIPTION
72XXA-010	Internal Battery Pack
72XXA-112	TCXO (2 ppm)
72XXA-131	Low Power Oven Time Base
72XXA-132	Superior Low Power Oven Time Base
72XXA-521	Data Output Unit
72XXA-522	Interface PCB Assembly
72XXA-529	IEEE Interface

Table 1-2. 7250A Accessories

MODEL NO.	DESCRIPTION
Y2014	C Size Single Unit Offset Rack Mount
Y2015	C Size Dual Rack Mount
Y2020	C Size Panel Mount
Y7201	Filter/Attenuator
Y7203	Instrument Cable, 2 ft.
Y7204	Instrument Cable, 5 ft.

Table 1-3. 7250A Specifications

GENERAL	
Display Annunciation	7-digit LED, Leading Zero Suppression sec, msec, μsec, kHz, MHz, Gate, Oven, Overflow.
Autorange	A 20 % hysteresis switching threshold eliminates redundant up/down resolution changes. Hysteresis can be reset by pressing the RESET switch.
Reset	Reset switch clears display, lights all display segments; on release, a new measurement is activated.
Cycle Rate	250 ms fixed between readings.
Operating Temperature	0° – 40°C
Operating Temperature (stacked)	0° – 40°C.
Storage Temperature	–40° – +70°C.
Power Requirements	23 VA.
Line Voltage	100, 120, 220 or 240V ac.
Line Frequency	47 – 63 Hz.
Dimensions	Standard type "C" PTI Case (See Figure 1-1) 10.49 cm H X 32.64 cm L X 20.45 cm W 4.13 in H X 12.85 in L. X 8.05 in W
Weight (without options)	2.7 kg 5 lbs. 15 oz.
FUNCTIONS **(see footnotes for definition of terms)**	
Frequency A	
Range	5 Hz – 80 MHz
Resolution	.1 Hz – 10 kHz in decade steps
Accuracy	±1 count ±time base errors
Display	kHz or MHz with decimal point
CPM X100A	
Range	5 Hz – 80 MHz
Resolution	100 CPM, fixed
Accuracy	±1 count ±time base errors
Display	No decimal point or annunciator
Ratio A/B	
Range	A: 5 Hz – 80 MHz B: 5 Hz – 1 MHz
Resolution	N X A/B
Accuracy	±1 count $\pm\frac{\text{(Freq A X Trig Error B)}}{N}$
Display	Decimal point without annunciator

Table 1-3. 7250A specifications (cont)

FUNCTIONS (cont)	
Period A	
Range	5 Hz – 1 MHz
Resolution	100 ns – 10 ms in decade steps
Accuracy	±1 count ±time base errors ±trig error
Display	msec or sec with decimal point
Period Average A	
Range	5 Hz – 1 MHz
Resolution	100 ns – 1 ps in decade steps
Accuracy	$\frac{\pm 100\text{ ns}}{N}$ ±time base error ±$\frac{\text{trig error}}{N}$
Display	μsec or msec with decimal point
Time Interval A/B	
Range	5 Hz – 2 MHz
Resolution	100 ns – 10 ms in decade steps
Accuracy	±100 ns ±time base errors ±trig error
Display	msec or sec with decimal point
Totalize A	
Range	5 Hz – 80 MHz
Count Capacity	0 – 9999999
Display	No decimal point or annunciator
STANDARD TIME BASE (10 MHz)	
Aging Rate per Month	$\pm 5 \times 10^{-7}$
Stability (0° – 50°C)	$\pm 5 \times 10^{-6}$
Line Voltage (±10%)	$\pm 1 \times 10^{-7}$
Battery	$\pm 1 \times 10^{-7}$

OPTION TIME BASE (10 MHz)

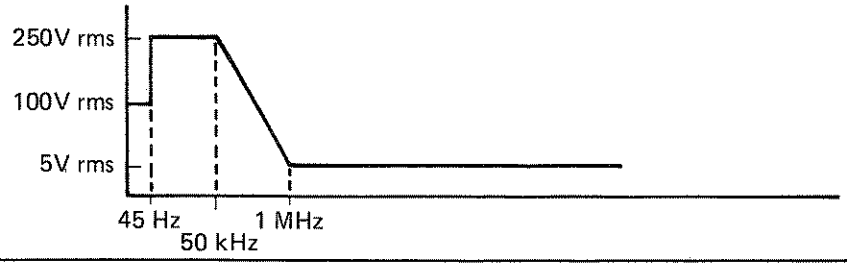
Aging Rate (constant temperature)	TCXO (2 ppm) Option -112	Low Power Oven Option -131	Superior Low Power Oven Option -132
per Day			$\pm 3 \times 10^{-9}$
per Month	$\pm 3 \times 10^{-7}$	$\pm 1 \times 10^{-7}$*	$\pm 5 \times 10^{-8}$*
per Year	$\pm 1 \times 10^{-6}$		
Accuracy with Temperature**			
(0 – 50°C)	$\pm 2 \times 10^{-6}$	$\pm 1 \times 10^{-7}$	$\pm 3 \times 10^{-8}$
Line Voltage (±10%)	$\pm 2 \times 10^{-8}$	$\pm 2 \times 10^{-8}$	$\pm 4 \times 10^{-9}$
Battery	$\pm 2 \times 10^{-8}$	$\pm 5 \times 10^{-8}$	$\pm 1 \times 10^{-8}$
Warmup***			
10 Min		$\pm 5 \times 10^{-7}$	$\pm 5 \times 10^{-7}$
20 Min		$\pm 3 \times 10^{-8}$	$\pm 3 \times 10^{-8}$

* After 5 days continuous operation.

** Accuracy with temperature includes errors caused by temperature variations during operation as well as all calibration errors.

*** This specification defines how close the oscillator will be to the final frequency within the specified time.

Table 1-3. 7250A Specifications (cont)

SIGNAL INPUTS – CHANNEL A & B	
Bandwidth	AC: 5 Hz - 80 MHz Channel B not used above 2 MHz
Sensitivity	10 mV rms (5 Hz – 50 MHz) 15 mV rms (50 – 80 MHz)
Attenuation	X1 to X100, continuously adjustable
Input Impedance	1 MΩ, shunted by less than 50 pF.
Filter (3 dB point)	100 kHz, low pass
Trigger Level	+150 mV, 0V, – 150 mV (fixed)
Maximum Input Voltage	
EXTERNAL TIME BASE INPUT	
Frequency Required	10 MHz, AC Coupled
Sensitivity	300 mV rms
Input Impedance	Nominally 1 kΩ in parallel with 30 pF
Maximum Input	3V rms

FOOTNOTES:

1. *$N = 10^0$ to 10^5 in decade steps set by resolution switch. Indicates the number of periods averaged in Period Average mode, and the number of cycles of B averaged in Ratio mode.*

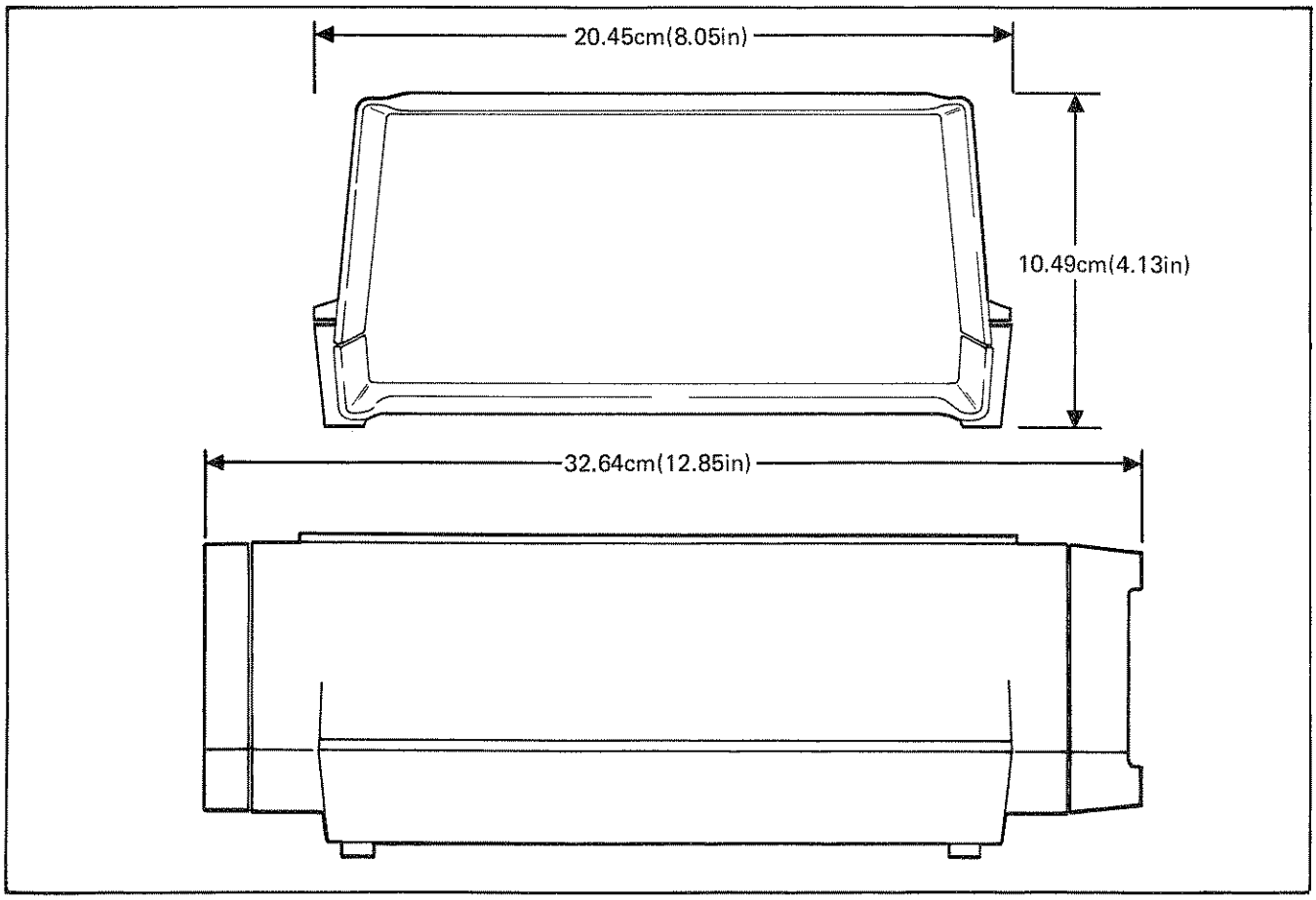
2. *Time base error is the sum of all errors specified in the time base section for a particular time base.*

3. *Trigger error is the measurement error caused by noise on the input signal triggering the input amplifier early or late. It is calculated as follows:*

$$\text{Trigger error} = \pm \frac{2X \text{ noise peak (V)}}{\text{signal slope at trig point V/}\mu s} \ \mu s$$

Table 1-3. 7250A Specifications (cont)

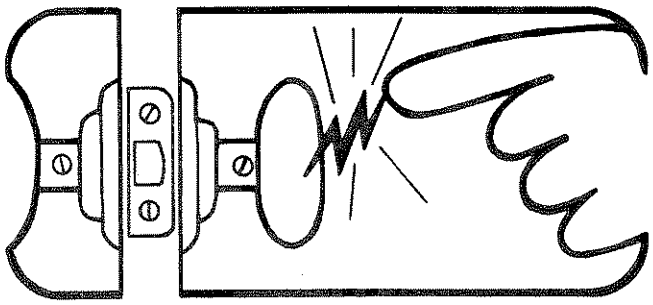
BATTERY PACK (OPTION –010)	
Operating Time	3.25 hours typical, continuous. Decrease to 3.0 hours with Option -131 or -132 oven oscillators installed.
Charge Time	16 hours at room temperature
Battery Type	Ni-cad, F cells
Charge Protection	Thermistor actuated shut down of charging circuit if battery temperature exceed 65°C.
Discharge Protection	Automatic low-voltage shut-down to prevent over discharge
DATA OUTPUT UNIT (OPTION -521)	
Description	Serial BCD output of all digits and annunciators
Levels	TTL, "1" state low
Speed	60 readings/sec
IEEE INTERFACE (OPTION -529)	
Description	Option for interfacing the 7250A to IEEE-488. Option package consists of a board in the 7250A, a ribbon cable and a board for the Fluke 1120A IEEE Translator. The 1120A must be used to interface 7250A to IEEE-488.
Function	Talker only
IEEE Repertoire	SH1, AH1, TE0, L4, LE0, SR1, RL2, PP0, DC1, DT1. C0



static awareness

A Message From

John Fluke Mfg. Co., Inc.

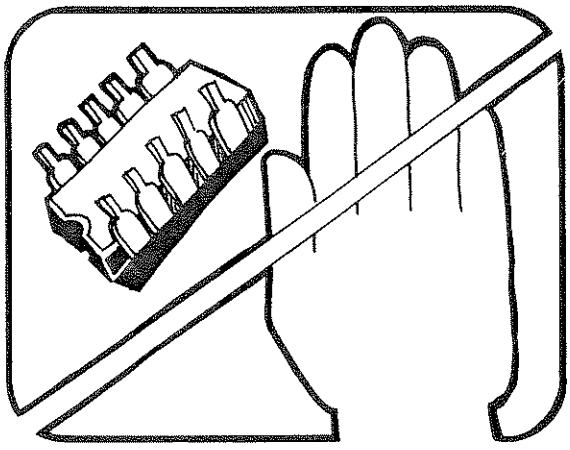


Some semiconductors and custom IC's can be damaged by electrostatic discharge during handling. This notice explains how you can minimize the chances of destroying such devices by:

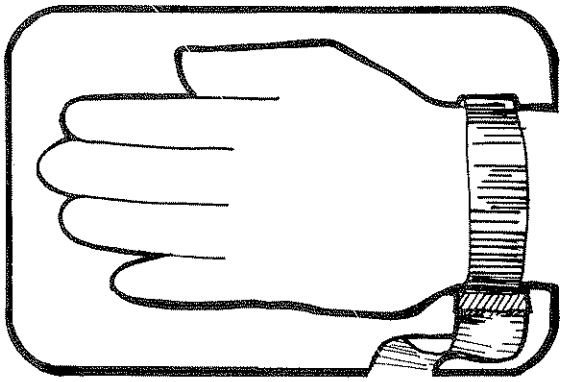
1. Knowing that there is a problem.
2. Learning the guidelines for handling them.
3. Using the procedures, and packaging and bench techniques that are recommended.

The Static Sensitive (S.S.) devices are identified in the Fluke technical manual parts list with the symbol "⊗".

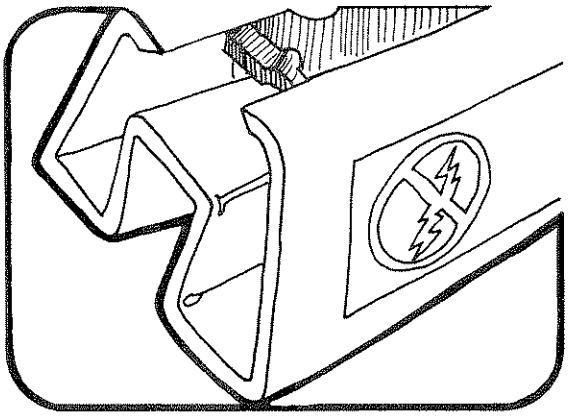
The following practices should be followed to minimize damage to S.S. devices.



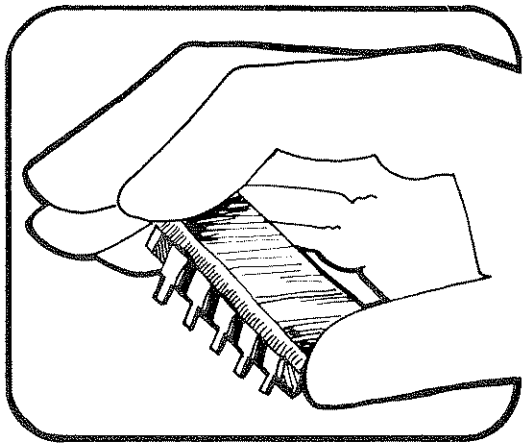
1. MINIMIZE HANDLING



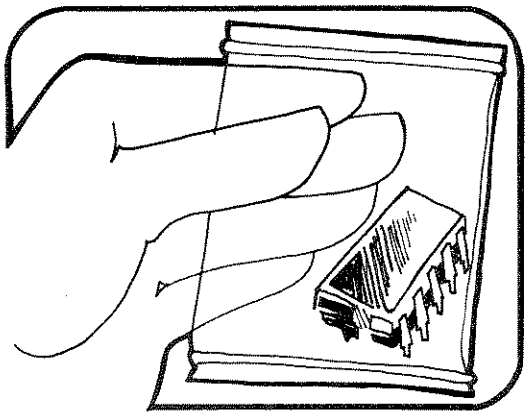
3. DISCHARGE PERSONAL STATIC BEFORE HANDLING DEVICES



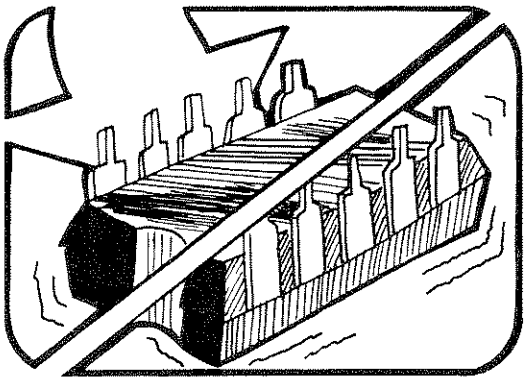
2. KEEP PARTS IN ORIGINAL CONTAINERS UNTIL READY FOR USE.



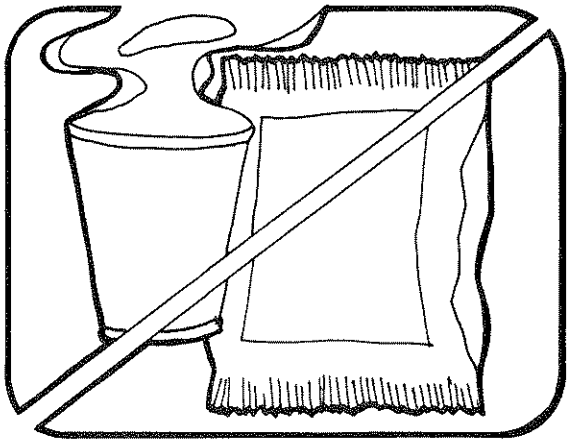
4. HANDLE S.S. DEVICES BY THE BODY



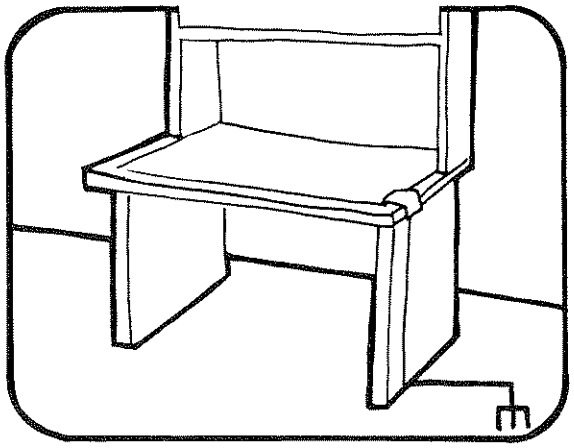
5. USE ANTI-STATIC CONTAINERS FOR HANDLING AND TRANSPORT



6. DO NOT SLIDE S.S. DEVICES OVER ANY SURFACE



7. AVOID PLASTIC, VINYL AND STYRAFOAM IN WORK AREA



8. HANDLE S.S. DEVICES ONLY AT A STATIC-FREE WORK STATION

9. ONLY ANTI-STATIC TYPE SOLDER-SUCKERS SHOULD BE USED.

10. ONLY GROUNDED TIP SOLDERING IRONS SHOULD BE USED.

Anti-static bags, for storing S.S. devices or pcbs with these devices on them, can be ordered from the John Fluke Mfg. Co., Inc.. See section 5 in any Fluke technical manual for ordering instructions. Use the following part numbers when ordering these special bags.

John Fluke Part No.	Bag Size
453522	6" x 8"
453530	8" x 12"
453548	16" x 24"
454025	12" x 15"

Section 2
Operating Instructions

2-1. INTRODUCTION

2-2. Installation and operation of the 7250A Universal Counter-Timer are explained in this section. Read this information before attempting to operate the unit. Should any difficulties arise, contact your nearest Fluke Sales Representative (listed in Section 7), or the John Fluke Mfg. Co., Inc., (P.O. Box 43210, Mountlake Terrace, WA., 98043; Telephone 206 774-2211).

2-3. SHIPPING INFORMATION

2-4. The 7250A is packaged and shipped in a foam-packed container. An Instruction Manual and any accessories ordered will be included with the instrument. Upon receipt of the instrument, make a thorough inspection for proper contents and possible shipping damage. Special instructions for inspection and claims are included with the shipping container. If reshipment is necessary, use the original container. If the original container is not available, a new container can be obtained from the John Fluke Mfg. Co., Inc. Please reference the instrument model number when requesting a new shipping container.

2-5. INSTALLATION

2-6. Input Power

2-7. The 7250A can be operated with an input line voltage of 100, 120, 220, or 240V ac (±10%). Line frequency may vary between 47 and 63 Hz. Before connecting the power cord, verify that line voltage switches (located inside the instrument) are properly set and that an appropriate line fuse is installed. Refer to Section 4 of this manual for proper verification procedures (See "Line Voltage Selection" and "Fuse Replacement").

2-8. Instrument Case Mating

2-9. The 7250A is contained in a molded instrument case with non-marring feet, a tilt-down bail, and a latching arrangement. This instrument may be stacked and latched together with other Fluke instruments employing this type of case.

2-10. Use the following procedure when attaching these molded cases together:

1. For the top instrument, pull out latches found on either side (refer to Figure 2-1).
2. Nestle top and bottom instruments together.
3. Push latches in to secure instruments together.

CAUTION

Instrument stacks should be limited to a total height of three feet and a total weight of 40 pounds.

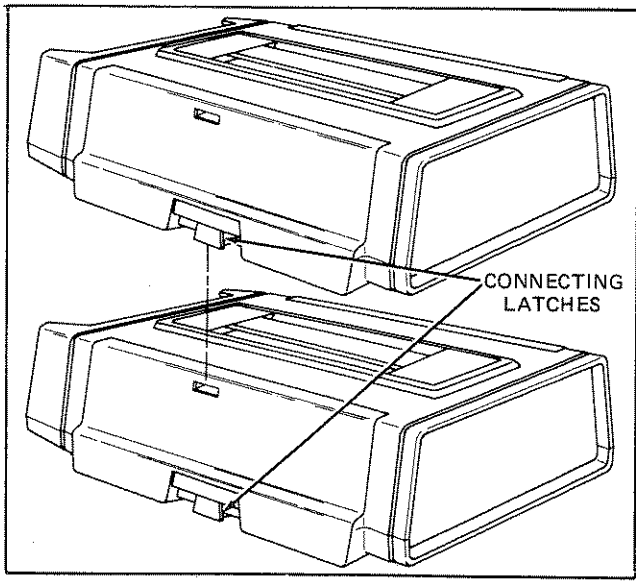


Figure 2-1. Instrument Case Mating

2-11. Tilt-Down Bail

2-12. When used as a separate instrument, the 7250A may be tilted up, or down, with the aid of the tilt bail. When extended, the bail may be locked in place by firmly pressing the legs into slots provided in the bottom panel. When retracted, the bail lies flush with the instrument's bottom panel and does not interfere with case mating. This bail will normally be mounted toward the front of the instrument's bottom panel. To remove the bail, compress either of its legs toward the center of the case and pull out. Installation may then be made in identical mounts at the rear of the bottom panel.

2-13. Rack Installation

2-14. The 7250A may be installed in a standard 19-inch equipment rack or a DIN panel mount. Mounting kits for these accessories are described in Section 6 of this manual. A list of all available accessories and options is presented in Section 1.

2-15. OPERATING FEATURES

2-16. The location of front panel controls, indicators and connectors is shown in Figure 2-2. Referenced by number, these items are briefly described in Table 2-1. Rear panel controls and connectors are covered in a similar fashion in Figure 2-3 and Table 2-2. It is suggested that the operator become acquainted with this information before operating the instrument.

2-17. OPERATING NOTES

2-18. The following paragraphs describe various conditions and information which should be considered before operating the Model 7250A Counter-Timer.

Table 2-1. 7250A Front Panel Controls, Indicators and Connectors

REF. NO.	NAME	FUNCTION
1	Gate Indicator	LED flashes at discernible rate to indicate gating in progress. Continuously cycles for FREQ A, CHK, CPM X100A. Constant illumination in TOT A. Input dependent for RATIO A/B, PER A, PER AVG A, TI A-B.
2	Overflow Indicator	LED illuminates when capacity of the display has been exceeded.
3	Oven Indicator	LED lights to indicate oven oscillator Options -131 or -132 are powered. Oscillator is powered whenever the 7250A is connected to ac or dc power (independent of the power control - #18). Rear panel selector switch must be in INT to power oven.
4	Display	Seven-digit readout displays measurement result with decimal point.
5	Units Annunciator	One of five LED's will light to define measurement units. (MHz or kHz in FREQ A or CHK; μsec, msec or sec in PER A, PER AVG A or TI A-B; no annunciator for CPM, RATIO or TOT.) LED illuminated is dependent on RESOLUTION.
6	CHANNEL A Slope and Variable ATTENUATION Control	Dual function control provides Channel A triggering on negative slope (in) or positive slope (out); also acts as variable attenuation in conjunction with X1 X10 control.
7	Attenuation Range Control (Channel A)	Slide switch selects range for variable attenuation control (#6). Ranges are X1 - X10 (X1) or X10 - X100 (X10).
8	CHANNEL B Slope and Variable ATTENUATION Control	Performs same function as #6, but for Channel B.
9	Attenuation Range Control (Channel B)	Performs same function as #7, but for Channel B.
10	Channel B Trigger Offset Control	+150 mV (⎍), 0V (∿) or −150 mV (⎏).
11	CHANNEL B Input Connector	BNC connector accepts 5 Hz to 80 MHz (250 mA maximum).
12	Separate/Common Control	When set to COM, the CHANNEL A input is routed to both Channel A and Channel B amplifiers, the CHANNEL B X1 X10 control is disabled, and the CHANNEL B input connector is disconnected. When set to SEP, CHANNEL A and B inputs are isolated.
13	FILTER Control	When IN, activates 100 kHz low pass filter for both channels.
14	CHANNEL A Input	BNC connector accepts 5 Hz to 80 MHz.

Table 2-1. 7250A Front Panel Controls, Indicators and Connectors (cont)

REF. NO.	NAME	FUNCTION
15	CHANNEL A Trigger Offset Control	Sets Channel B trigger level at +150 mV (⎍), 0V (∿), or −150 mV (⎏).
16	FUNCTION Control	Slide switch selects operating function: FREQ A measures frequency of CHANNEL A input (5 Hz - 80 MHz); CPM X100A displays counts per minute scaled by 100 with input from appropriate transducer (i.e., 25 is displayed for a 2500 count input); RATIO A/B displays Channel A input frequency divided by Channel B input frequency; PER A measures the elapsed time of one input cycle on Channel A (5 Hz - 1 MHz); PER AVG A measures average elapsed time of multiple cycles of signal on Channel A; TI A-B measures elapsed time between Channel A and Channel B input signels; TOT A displays the total counts accumulated in CHANNEL A; CHK verifies count and display circuits by disabling inputs and reading out 10 MHz clock frequency.
17	RESOLUTION Control	Slide switch determines displayed resolution and annunciator selection for each function. Top range (N) defines number of periods averaged in PER AVG A, RATIO A/B. Middle range (100 ns - 10 ms) defines least significant digit resolution in PER A and TI A-B modes. Bottom range (10 kHz - 0.1 Hz) defines resolution of least significant digit in FREQ A and CHK modes.
18	RESET Control	Resets display and initiates a new measurement cycle. Lights all display segments when held depressed.
19	Battery Select	Selects battery operation (push in) when Battery Option -010 is installed.
20	Power Control	Push ON/push STBY.

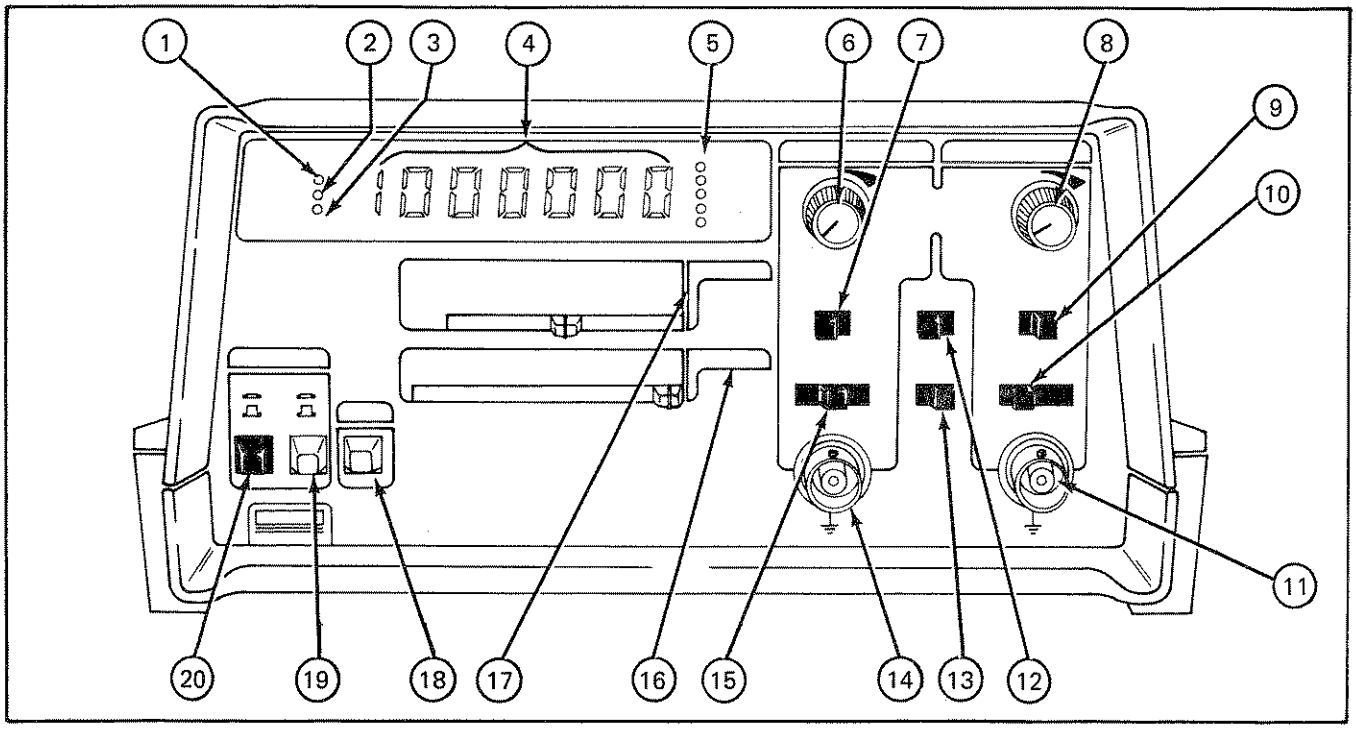


Figure 2-2. 7250A Front Panel Controls, Indicators and Connectors

Table 2-2. 7250A Rear Panel Controls and Connectors

REF. NO.	NAME	FUNCTION
1	Line Power Receptacle	Receives three-prong power cord with offset prong attached to earth ground.
2	Line Fuse	Fuse access; refer to Section 4 when replacing the line fuse.
3	Data Output Connector	Connector for Data Output Option -521 accessible here.
4	10 MHz REF In	BNC connector for externally sourced 10 MHz reference.
5	Reference Select Control	Slide switch selects source for 10 MHz reference frequency. In EXT, the 7250A will use the 10 MHz signal present at the 10 10 MHz REF In BNC in place of the internal time base. Power to the internal time base will be disconnected and any internal oven time base will cool. In INT, the instrument uses the internal time base; the frequency from this time base will then be available at the 10 MHz REF In BNC.

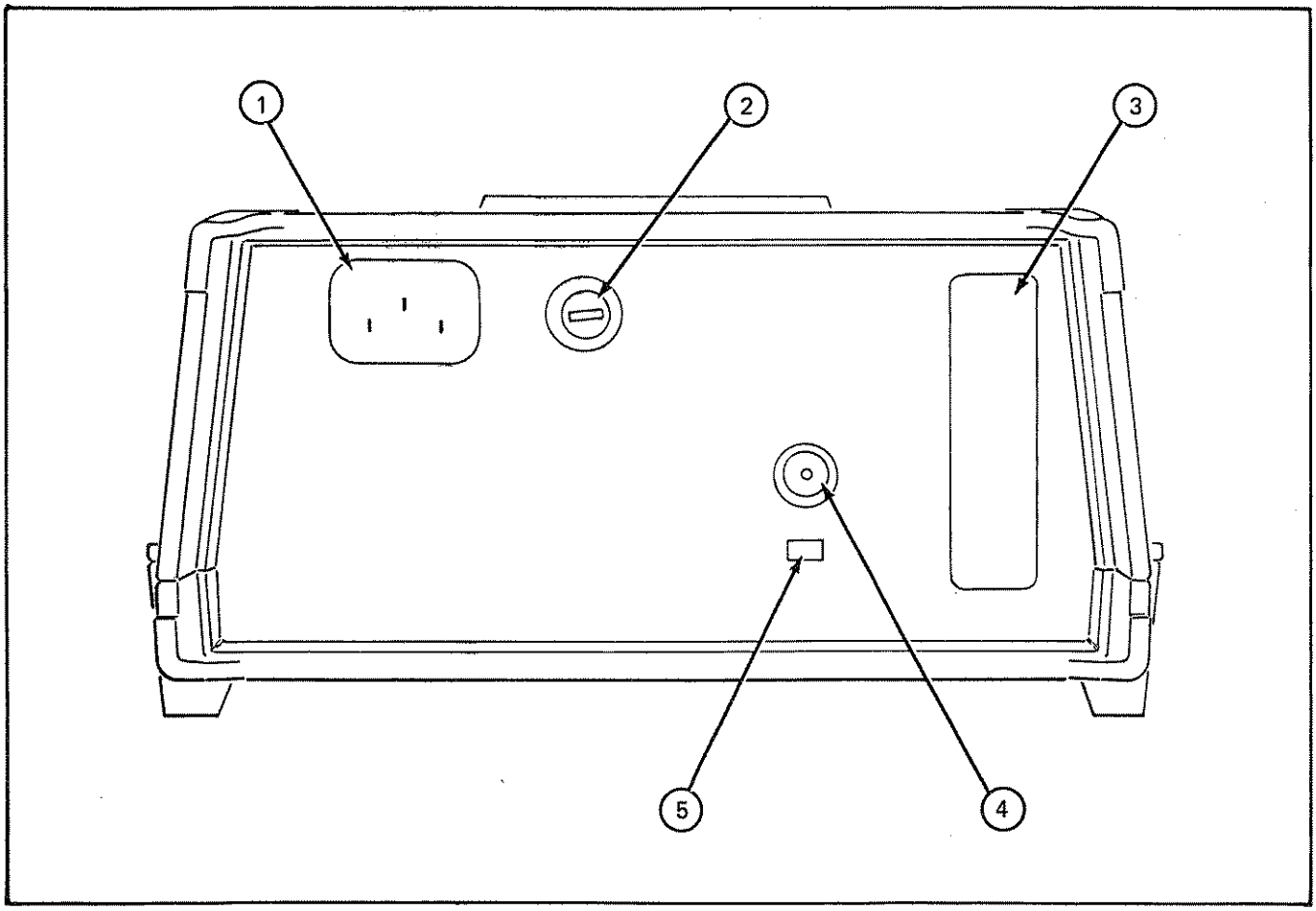


Figure 2-3. 7250A Rear Panel Controls and Connectors

2-19. AC Line Connection

2-20. The input power cord is a three-pin polarized connector which permits connection to any of the power voltages described in INPUT POWER. Ensure that the ground pin is connected to a high quality earth ground.

2-21. Maximum Inputs

WARNING

ALL BNC CONNECTOR SHELLS ON THE 7250A ARE TIED DIRECTLY TO EARTH GROUND THROUGH THE POWER PLUG. DO NOT CONNECT THE ACTIVE LEAD OF THE INPUT SIGNALS TO THE SHELL. IRREPARABLE DAMAGE TO THE INSTRUMENT OR THE SIGNAL SOURCE MAY RESULT.

2-22. Table 2-3 defines the maximum allowable signal level input for each input terminal. Channels A and B are fuse protected (250 mA). Refer to Section 4 of this manual for fuse replacement instructions.

2-23. Counter-Timer Terminology

2-24. The following definitions are useful in understanding how and when to use the 7250A's controls.

25. ATTENUATION

2-26. Attenuation is used to limit the input signal within the input amplifier's linear range. On the 7250A, two attenuation controls for each channel are provided to limit the input amplifier's gain. The X1 X10 control, in combination with the variable attenuation control, provides continuous attenuation in two ranges (X1-X10, X10-X100).

2-27. CYCLE RATE

2-28. This term refers to the minimum time necessary for the instrument to process and display a measurement. It does not include the actual measurement time. In the 7250A, each cycle time is 250 ms.

Table 2-3. Maximum Inputs

CHANNEL A	250V rms to 50 kHz, varying down to 5V rms at 1 MHz and above.
CHANNEL B	Same as A.
EXT REF	3V rms.

2-29. DISTORTION

2-30. Distortion refers to an unwanted change in the input waveform. It may occur at equally spaced (harmonic) or random (non-harmonic) intervals.

2-31. DUTY CYCLE

2-32. Duty cycle specifies the ratio of signal on time to off time. The greater the percentage of off time, the lower the duty cycle. With AC-coupled inputs, such as on the 7250A, low duty cycle signals will not be properly coupled to the input amplifier; the Trigger Offset control can be used to alleviate this situation.

2-33. EVENT COUNTING

2-34. The accumulation of a number of events over a period of time is termed event counting. Several 7250A functions perform this operation. The FREQ A mode counts events for a specific length of time to determine the Channel A input frequency. In the CPM mode, the Channel A input frequency is counted in the same manner; a conversion factor is now used to normalize the frequency (counts per second) into counts per minute. In TOT A mode, events are counted and displayed continuously on Channel A. Finally, in RATIO A/B mode, the 7250A will count events on Channel A during a gate time determined by the signal on Channel B. The instrument can measure events generated by a wide variety of sources. For example, the FREQ A function can be used to measure the precision frequency output of a signal synthesizer, and the CPM function can be used to determine the rotational speed of a conveyor belt spindle.

2-35. When using any function that counts events, the instrument must trigger once, and only once for each event. Use of the front panel controls must be directed toward this end. Noise must be filtered or attenuated to prevent false triggering, and the input signal must be kept within the linear range of the instrument.

2-36. EVENT TIMING

2-37. During event timing functions, an internal oscillator frequency is counted for a period determined by the input signal. In the 7250A, two types of event timing measurements can be made: period and time interval. Period measurement (PER A or PER AVG A) determines the period, or inverse of frequency, of a repetitive signal. The instrument measures period by counting an internal oscillator's frequency for single (PER A) or multiple (PER AVG A) cycles of the input. Time interval measurements (TI A-B) can be made to determine the period of time between any two events, repetitive or not. For either type of event timing, separate start and stop signals must be generated from the input (refer to Figure 2-4).

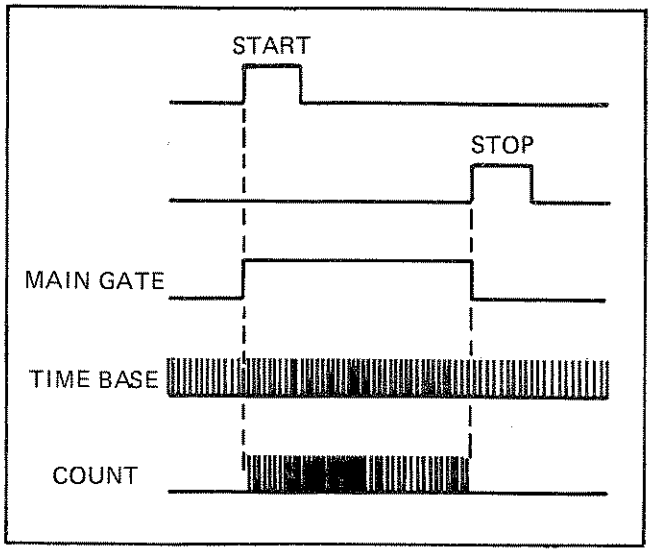


Figure 2-4. Event Timing

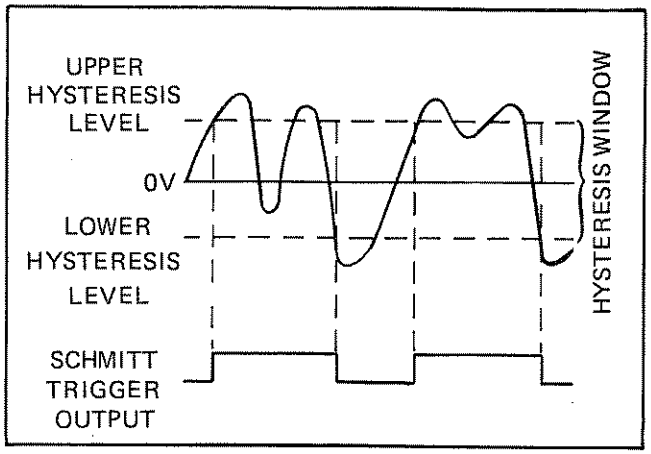


Figure 2-5. Hysteresis Window

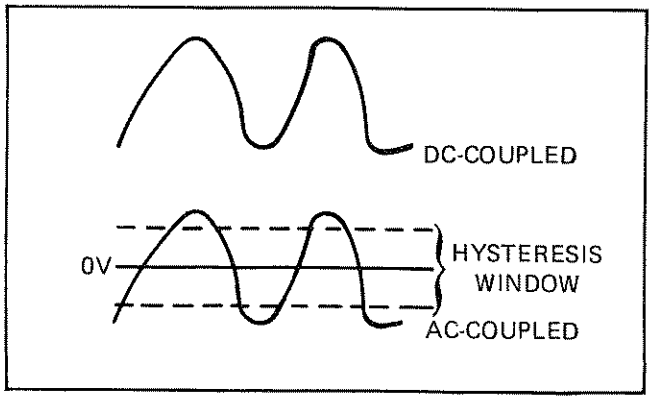


Figure 2-6. AC/DC Input Coupling

2-38. GATE TIME

2-39. Gate time refers to the length of time during which a frequency is being counted for display. The frequency counted may be derived from the input signal or from the instrument's internal time base. With longer gate times, more counts are accumulated and measurement resolution improves.

2-40. HYSTERESIS

2-41. In instruments such as the 7250A, proper counting and timing requires a pulsed output from the input circuitry. To form this pulse, each input waveform (regardless of its shape) triggers the input circuitry on or off at predetermined triggering, or hysteresis levels. An input waveform must pass through both of these hysteresis levels for the input circuitry to generate a pulse. The voltage difference between the two levels is termed the hysteresis window; the minimum signal that can trigger both levels therefore defines the instrument's sensitivity. Generation of the hysteresis window is illustrated in Figure 2-5.

2-42. INPUT COUPLING

2-43. Either ac or dc coupling may be used to transfer the input signal to the input conditioning circuitry. As illustrated in Figure 2-6, a large dc component can shift an input signal away from the hysteresis levels necessary for proper triggering. In the 7250A, both channel inputs are therefore ac-coupled.

2-44. INPUT IMPEDANCE

2-45. The input impedance defines the impedance seen by a signal source. Impedance for each channel in the 7250A is 1 MΩ shunted by 50 pF. This arrangement allows for measurements in the specified frequency range without source loading and resultant waveform distortion or attenuation.

2-46. LINEAR OPERATING RANGE

2-47. The linear operating range refers to the excursions of the input signal that can reliably trigger the input amplifier without distortion. The 7250A's linear range varies between the smallest signal level acceptable by the input amplifier (minimum) and the largest attenuated signal that will not be clamped by the amplifier's input circuits (maximum). The minimum is defined by the instrument's sensitivity specifications. Operation within maximum levels may be ensured through proper use of the ATTENUATION controls. Exceeding the input amplifier's linear range will probably not cause false counting; saturation effects may, however, decrease both input impedance and frequency response, causing waveform distortion.

2-48. NOISE

2-49. Noise is defined as spurious signals riding on the input waveform. Unlike distortion, the waveform is not changed. Noise of sufficient amplitude can, however, cause false triggering, resulting in inaccurate measurements during event timing functions. The 7250A

input amplifiers (signal conditioners) exhibit very low noise. The signal applied to these amplifiers may, however, be plagued with noise from the signal source, the electrical environment or from improper signal transfer to the 7250A.

2-50. ONE COUNT ERROR

2-51. The one count ambiguity, inherent in any gate and counter type of frequency meter, results from an out-of-phase relationship between the input signal and the internal oscillator signal. The effect is demonstrated in Figure 2-7. During a one second gate time, the top 9.5 Hz signal accumulates a count of ten; during the same gate time, the phase-shifted bottom signal accumulates only nine counts. The ambiguity amounts to one displayed count.

2-52. RESOLUTION

2-53. This term defines the value of the smallest displayed unit in a measurement. In the 7250A, this unit (the least significant digit, or LSD) is defined by each combined setting of the FUNCTION and RESOLUTION controls.

2-54. SENSITIVITY

2-55. Sensitivity defines the smallest signal amplitude capable of triggering the instrument. This specification corresponds to an rms value of the peak-to-peak difference between hysteresis levels (the hysteresis window). Note that the waveform must pass both hysteresis levels before a count is generated from the input circuitry; false triggering from noise or distortion on the input signal is thereby minimized.

2-56. TIME BASE ERROR

2-57. Time base error stems from crystal aging, temperature variation, and line voltage fluctuation. The 7250A may be fitted with one of several available time base oscillators; specifications for each are included in Section 1 of this manual.

2-58. TRIGGER ERROR

2-59. Input signal irregularities (noise, distortion, etc.) may cause premature or delayed triggering at the input circuitry's hysteresis levels. During event counting functions, this error is significant only when extra pulses are generated by the input circuitry. In event timing functions triggering error may be significant; improper triggering translates into inaccurate counting of the internal oscillator frequency. Figure 2-8 illustrates possible trigger errors.

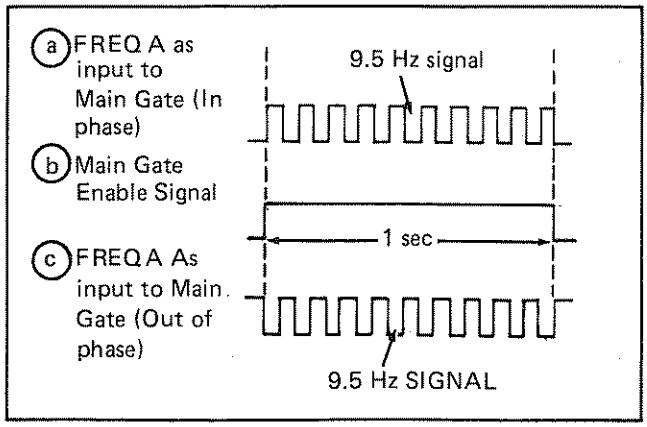


Figure 2-7. One Count Error

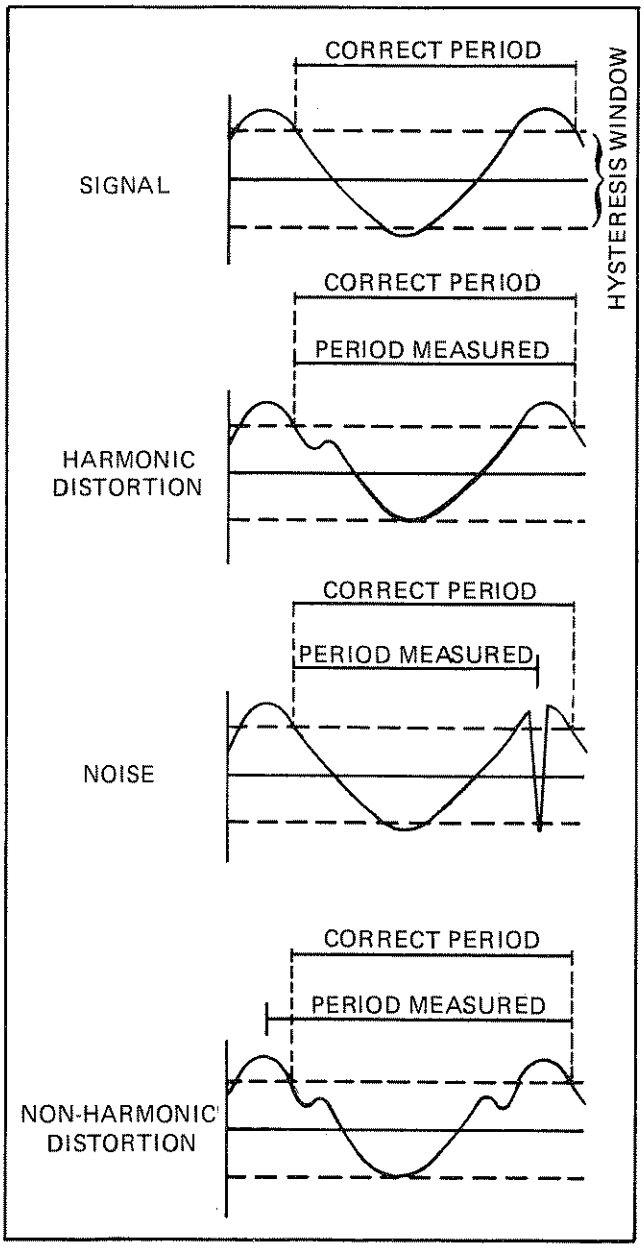


Figure 2-8. Trigger Error in Event Timing

2-60. TRIGGERING

2-61. Signal conditioning circuits ideally provide a pulse train output representative of the input signal. These pulses occur at the same frequency in Event Counting functions; they signify start or stop times in Event Timing functions. Each pulse is triggered on and off at the specified upper and lower hysteresis levels for the instrument.

2-62. TRIGGER LEVEL

2-63. The voltage level nominally halfway between upper and lower hysteresis levels is termed the trigger level. On the 7250A, one of three fixed trigger levels may be selected with the Offset control. The ATTENUATION controls can then by used to limit the input signal within the instrument's linear range.

2-64. Function Control

2-65. The FUNCTION slide switch selects any of the available functions. Each change generates an internal reset. OPERATING DIRECTIONS provide descriptions, operating limits, and specific procedures for each function.

2-66. Resolution Control

2-67. The front panel RESOLUTION control selects autoranging or one of six manual ranges. Each of these settings is defined by three function-related scales. The scale used with FREQ A, PER A, PER AVG A, RATIO A/B, CHK or T.I. A-B is discussed with the appropriate OPERATING DIRECTION in this manual.

2-68. The RESOLUTION control will have no effect in two functions. For totalizing measurements (TOT A), resolution is set at the least significant integer. In the counts per minute mode (CPM X100A), resolution is determined by dividing the number of counts per revolution by the number of minutes. If a 100 count-per-revolution input is used, resolution will translate directly to one RPM.

2-69. When placed in AUTO, the 7250A will automatically step through a predetermined series of resolution settings. The settings available for each function are defined in Table 2-4. When autoranging, the instrument seeks the greatest resolution possible, without overflow, for the function selected and the signal being measured. As an example, with FREQ A selected, the 7250A will step through all five available resolutions to maximize its display capacity when measuring a frequency of 1.2 MHz: the reading will be "1200.000 kHz". If 1200 Hz is measured, maximum resolution allowable will again be found at the last step, but the reading will be "1.200 kHz". Once a resolution is set, frequency variations of up to 20% will be tolerated without further resolution changes.

NOTE

During autoranging in the PER A mode, the GATE LED may flash more than once for each display update.

2-70. Separate/Common Control

2-71. The SEP/COM control is used to select the input to the Channel B amplifier. In SEP, the Channel B input

Table 2-4. Autoranging

	10^0 10 kHz	10^1 1 kHz	10^2 100 Hz	10^3 10 Hz	10^4 1 Hz	10^5 0.1 Hz
FREQ A	———	———	———	———	———	
RATIO A/B		———	———	———	———	———
PER A	———	———	———	———		
PER AVG A	———	———	———	———	———	
TI A-B	———	———	———	———		
CHK	———	———	———	———	———	

(Autoranging not used in TOT A or CPM X100A)

connector is tied to the Channel B amplifier. In the COM position, the Channel A input connector is tied to both the Channel A and B Amplifiers; the Channel A X1 X10 control now influences the signal to both amplifiers, while the variable ATTENUATION controls for Channel A and B still affect each input amplifier's gain individually.

NOTE

In COM, the Channel B input is not connected.

2-72. Attenuation Controls

2-73. Consisting of an X1 X10 switch and a variable control, ATTENUATION can limit instrument input circuit gain by factors of X1 (X1 switch position, fully ccw rotary position) through X100 (X10, fully cw) of the input. Large signals causing distortion or non-linear operation can therefore be reduced to within the instrument's linear range. Increased attenuation may also be used to compensate for noise on the input signal; use of ATTENUATION in this case can prevent the noise from crossing both of the hysteresis levels.

2-74. Slope Control

2-75. The slope control determines instrument triggering order; the initial trigger may occur on a negative going signal (control pushed in) or on a positive going signal (control pulled out). This control is part of the double function variable ATTENUATION control.

2-76. Filter Control

2-77. The position of the Filter IN/OUT switch determines whether or not frequencies above 100 kHz are removed from the input signal. When the control is at the IN position, the upper bandpass limit of the input amplifier on the Preamplifier is lowered from 80 MHz to 100 kHz. If high frequency noise is a problem with a low frequency signal, the 100 kHz low pass filter may be used to advantage.

2-78. Offset Control

2-79. The level of the triggering point, with respect to zero volts, is determined by the position of the Offset control. Figure 2-9 shows the position of the hysteresis window for each position of this control. The center position (shown in A) is optimum for symmetrical waveforms, (such as sine waves). Other waveforms, such as pulse signals with low duty cycles, will be biased by the ac-coupling circuit because of the relatively short charge time involved. These signals cannot be counted by the instrument with the control in the center position; the waveform fails to cross both levels of the hysteresis window. The other two positions of the control shift the position of the hysteresis window, with respect to zero volts, so that either negative or positive offset pulses can be counted.

2-80. Display

2-81. The 7250A display presents a seven digit LED readout with leading zero suppression. Measurement unit annunciators of MHz or kHz will be activated in FREQ A or CHK modes. For PER, PER AVG A, or T.I. A-B, annunciators for μsec, msec, or sec will illuminate. There will be no units annunciation in RATIO A/B, TOT A, or CPM X100A modes. Decimal point placement is determined by RESOLUTION and FUNCTION settings, as defined by Figure 2-10.

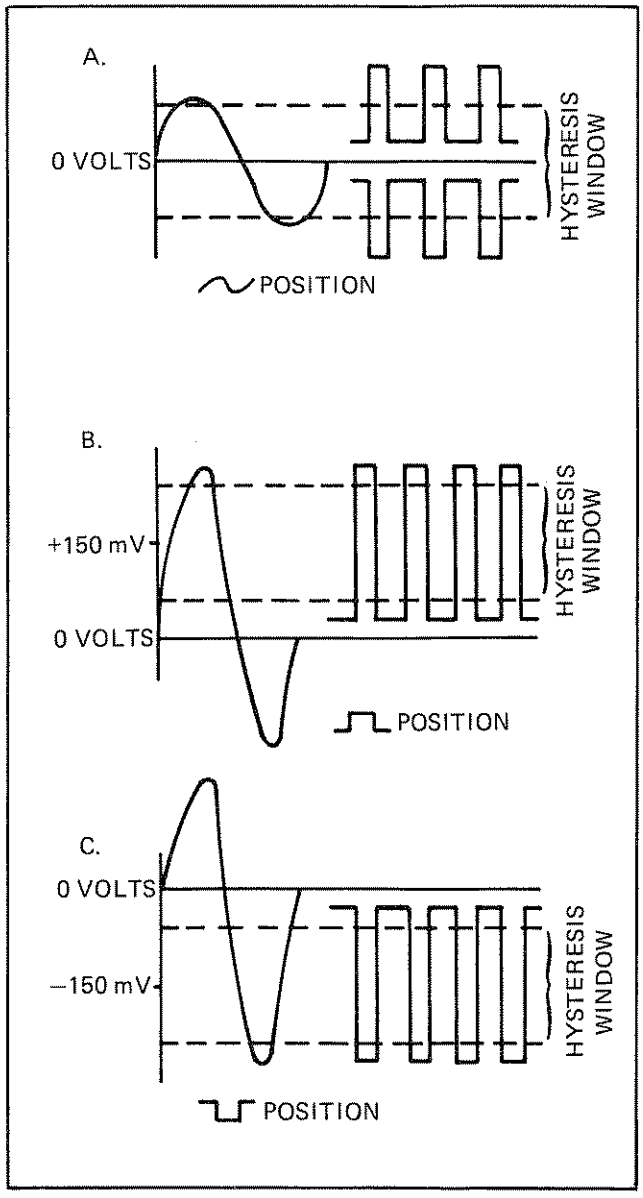
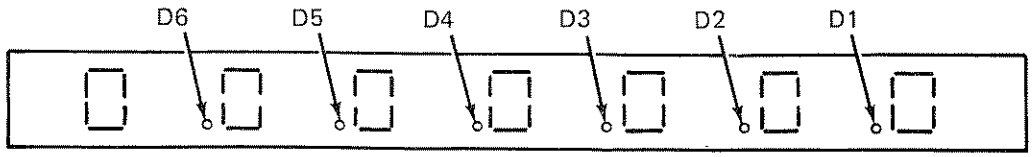


Figure 2-9. Trigger Level Control



	RESOLUTION						
	10^0	10^1	10^2	10^3	10^4	10^5	
	100 ns	1 μs	10 μs	100 μs	1 ms	10 ms	AUTO
	10 kHz	1 kHz	100Hz	10 Hz	1 Hz	0.1 Hz	
FREQ A	D2	D3	D4	D2	D3	D4	
RATIO A/B	–	D1	D2	D3	D4	D5	
PER A	D4	D3	D2	D4	D3	D2	
PER AVG A	D4	D5	D3	D4	D5	D6	
T.I. A–B	D4	D3	D2	D4	D3	D2	
CHK	D2	D3	D4	D2	D3	D4	

Figure 2-10. Decimal Point Identification

2-82. There are three status annunciators. The GATE annunciator provides an indication of counting or timing in progress. The OVFL annunciator will illuminate when the capacity of the internal seven-decade accumulator is exceeded. The OVEN annunciator should be on whenever an oven oscillator (Option -131 or -132) is installed and the instrument is connected to line or battery power (STBY or ON).

2-83. Accuracy

2-84. Techniques are available for improving the accuracy of any measurement. Even with the controls set for optimum performance, three error factors may degrade accuracy. These errors (one count error, trigger error, and time base error) relate to each function as defined in the following accuracy statements:

1. FREQ A
   ±1 count ±time base error

2. CPM X 100 A
   ±1 count ±time base error

3. RATIO A/B
   ±1 count A ± (FREQ A X trigger error B)

4. PER A
   ±1 count clock ±trigger error ±time base error

5. PER AVG A

   ±time base error $\quad \frac{(\pm 100 \text{ ns} \pm \text{trigger error})}{N}$

6. T.I. A.B.
   ±1 count clock ± trigger error
   ±time base error

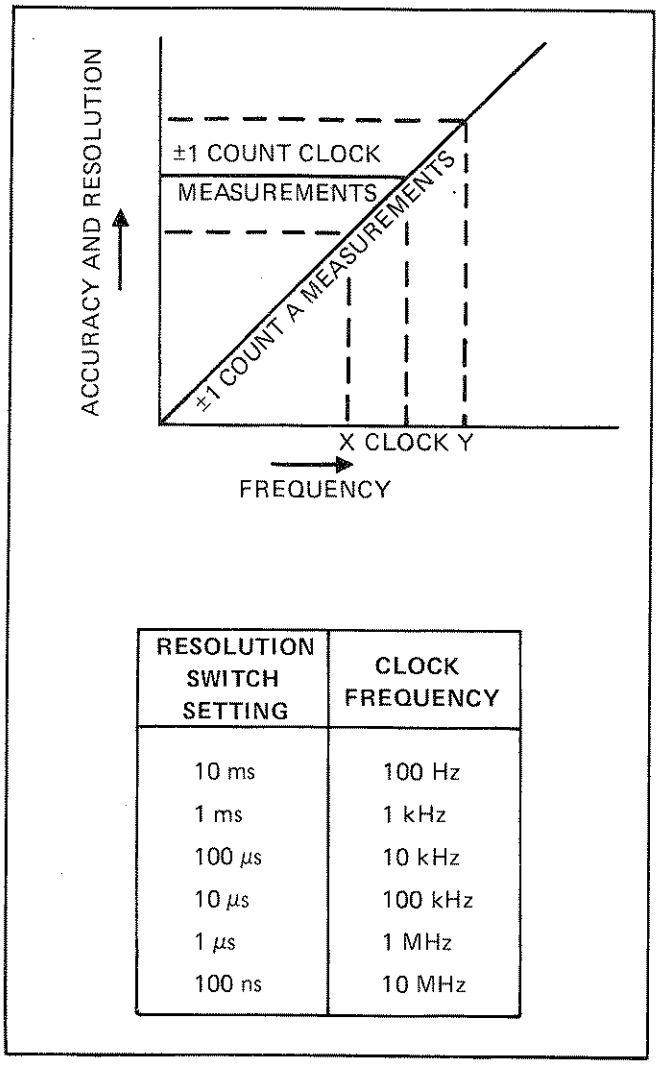
7. CHK
   ±1 count time base

2-85. Dealing with One Count Error

2-86. There are several methods available for reducing the effect of one count error. The following considerations may be useful:

1. By selecting a longer gate time, the percentage error caused by the ±1 count gate uncertainty is decreased.

2. The percentage accuracy of functions affected by ±1 count A depends upon the frequency of the input signal. As frequency increases, accuracy increases. As frequency decreases, accuracy decreases. The sloped line (±1 count A), in Figure 2-11, illustrates this concept. With a higher frequency input, more counts will be made per gate time, and ±1 count error will become less significant. The percentage error is thereby reduced.



RESOLUTION SWITCH SETTING	CLOCK FREQUENCY
10 ms	100 Hz
1 ms	1 kHz
100 μs	10 kHz
10 μs	100 kHz
1 μs	1 MHz
100 ns	10 MHz

Figure 2-11. Frequency Effect on Accuracy

3. FREQ A and PER A functions can be used selectively to maximize accuracy of frequency measurements over the range of Channel A. The relationship between the two measurement functions is shown in Figure 2-10. The following can be drawn by this function comparison.

a. FREQ A provides the best measurement accuracy if the input signal is higher in frequency than the instrument time base oscillator (10 MHz).

b. PER A provides the best measurement accuracy if the input signal is lower in frequency than the instrument time base oscillator.

4. When using these guidelines, the operator must exercise discretion. In a high noise environment, or where a great deal of non-harmonic distortion might be expected, gate time errors due to improper triggering may be significant; FREQ A might be the better choice regardless of the input signal frequency.

2-87. Reducing Time Base Error

2-88. Some of the effects of crystal related time base errors can be reduced. If the temperature of the instrument environment is maintained at a constant value, temperature error is minimized. If tight control of the instrument environment fails to produce the accuracy desired, the time base crystal related error can be reduced through recalibration or by substituting a time base with smaller errors. This time base may either be one of the optional internal time bases described in Section 6, or an external 10 MHz reference connected to the instrument via the rear panel.

2-89. Trigger Error Considerations

2-90. Improperly triggered hysteresis levels can cause error when using any function. When using ratio or event timing functions, trigger errors produce gate time errors, resulting in inaccurate displayed counts. Proper use of ATTENUATION and FILTER controls, along with other noise reduction techniques, will help solve this problem. In addition, the following considerations should be kept in mind:

1. Period measurements use Channel A for both START and STOP pulses; triggering errors are from one channel only. Trigger error will be caused by noise on the input signal. The period averaging function will reduce the effect of the triggering error by a factor of 1/N.

2. Time interval measurements use both Channel A and Channel B for the START and STOP pulses; the trigger error may arise from either or both channels.

3. In the Ratio mode, the counts of Channel B trigger error increase as the frequency of the Channel A input signal increases.

4. A pulse input signal, with faster rise times, will exhibit less trigger error than a sine wave input.

2-91. Reducing Errors due to Noise on the Input Signal

2-92. The following techniques may also be used to ensure noise rejection:

1. Use an oscilloscope to identify the presence of noise.

2. Use the variable and X10 ATTENUATOR controls to limit noise levels while maintaining sufficient signal levels for triggering.

3. Use an oscilloscope probe (X10) as the input cable when measuring high impedance circuits.

4. Use a low pass filter/attenuator. The front panel FILTER control can be utilized to attenuate signals above 100 kHz. Alternately, the Fluke Model Y7201 Filter/Attenuator, attached to the front panel input connector, can be used to suppress unwanted noise. This accesssory is described in Section 6 of this manual.

2-93. Summary

2-94. Some of the errors that affect accuracy are inherent and cannot be much improved without substituting different components (time base error). Accuracy can be improved by using the proper techniques (triggering error) or by selecting the correct function (PER A versus FREQ A). The accuracy of the event timing functions can be improved by using the appropriate averaging function. And, sometimes, the technique that decreases the effect of one error source increases the effect of another error source. Noise and distortion on the input signal or signals also affect the accuracy of measurement. The operator should be aware of all facets of the error sources and exercise discretion in using the instrument to make precise measurements.

2-95. OPERATING DIRECTIONS

2-96. Operation of the 7250A is spelled out for each function in the following paragraphs. Function capabilities, as well as useful operating hints, are also presented here.

2-97. Initial Procedure

2-98. The following procedural checks should be performed prior to using any of the function operating directions.

1. Check that the instrument has been connected to appropriate line power.

2. Ensure that the rear panel EXT-INT select switch is set to INT.

3. Press power to ON.

4. Ensure adequate time for instrument warmup, especially if an optional oven time base is installed (typically 10 minutes).

2-99. Frequency Measurements (FREQ A)

2-100. Frequencies on Channel A from 5 Hz through 80 MHz can be counted and directly displayed using this function. The gate times available range from 0.1 ms through 10s in six decade steps selectable with the RESOLUTION control (respective markings of the 10 kHz through 0.1 Hz). Input amplitudes should not exceed 250V rms from 45 Hz to 50 kHz (lowering to 5V rms at 1 MHz and above). Use the following procedure when making frequency measurements:

1. Set front panel controls as follows:

FUNCTION - FREQ A
RESOLUTION - as required, or AUTO
ATTENUATION - fully clockwise, X10
OFFSET CONTROL - set to ∿
SEP/COM - SEP
FILTER - OUT

2. Connect the signal to be measured to the CHANNEL A input connector.

3. Adjust the variable attenuation control counterclockwise until a stable display is seen. If this cannot be accomplished in the X10 range, return the variable control fully clockwise and change the range to X1. Now again reduce the variable attenuation (counterclockwise) until a stable display is seen.

4. Set the RESOLUTION control to obtain desired resolution of the displayed frequency. The OVFL annunciator will light if the display's capacity is exceeded.

NOTE

When dealing with low frequencies, period measurements yield greater accuracy.

2-101. Counts per Minute Measurements (CPM X100A)

2-102. The 7250A can be used as a tachometer to read out revolutions per minute. The input to Channel A in this function must be from a 100 pulse per revolution transducer. For transducers having other pulse per revolution rates, the 7250A readout can be converted to RPM with the formula:

$$[\text{RPM} = \text{readout X } \frac{100}{\text{pulses per rev.}}]$$

When the CPM X100A function is selected, gate time is set to 0.6s, the RESOLUTION control is disabled, and

the display will not indicate a decimal point or units annunciator. Use the following procedure when making counts per minute measurements:

1. Set front panel controls to:

   FUNCTION - CPM X100A
   SEP/COM - SEP
   OFFSET - as required
   ATTENUATION - fully clockwise, X10
   FILTER - out

2. Connect the transducer output to the CHANNEL A input connector.

3. Reduce ATTENUATION controls until a stable display is obtained.

NOTE

The output voltage from magnetic transducers will vary with speed of revolution. ATTENUATION controls may in such cases need to be readjusted. Alternately, a photo-electric transducer will provide an output level not dependent on frequency.

2-103. Ratio Measurement (RATIO A/B)

2-104. When using the RATIO A/B function, the instrument counts the frequency of input on Channel A and uses the frequency input on Channel B, instead of the reference frequency from the time base, to determine the length of gate time. The result is displayed without measurement units annunciation.

NOTE

The higher frequency must be input on Channel A.

2-105. The position of the Resolution control determines the number (N) of cycles of Channel B input signal that must be used to determine gate time. The 10^0-10^5 scale is used. As the Resolution control also causes positioning of the decimal point, automatic averaging of the number of counts of A accumulated during N cycles of B will occur.

2-106. Use the following procedure when making Ratio measurements:

1. Set front panel controls as follows:

   FUNCTION - RATIO A/B
   RESOLUTION - as desired, or AUTO
   SEP/COM - SEP
   FILTER - OUT
   ATTENUATION - fully clockwise, X10 (both channels)
   OFFSET CONTROL - set to ∿ (both channels)

2. Connect the higher of the two frequencies to CHANNEL A input connector. Momentarily place the FUNCTION control to FREQ A. Adjust the variable attenuation control (Channel A) counter clockwise until a stable display is seen. If this cannot be accomplished in the X10 range, return the variable control fully clockwise and change the range to X1. Now again reduce the variable attenuation (counterclockwise) until a stable display is seen. Return the FUNCTION control to RATIO A/B.

3. Connect the lower of the two frequencies to CHANNEL B input connector (5 Hz through 1 MHz).

4. Adjust Channel B ATTENUATION controls to ensure proper triggering (GATE LED flashing). Follow the techniques described for Channel A. Gating is derived from the CHANNEL B signal when in the Ratio function; generally, the greater the level of the signal on CHANNEL B, the greater the accuracy of the Ratio measurement will be.

5. Set the RESOLUTION control to obtain desired resolution of the ratio measurement.

2-107. Period Measurements (PER A)

2-108. This function can be used to measure the period of an input signal with frequencies from 5 Hz through 1 MHz.

2-109. The period function provides a great improvement in both accuracy and resolution of measurements made on low frequency signals. To make period measurements, the instrument measures the time interval between two consecutive cycles of a repetitive signal; Channel A is used to generate start and stop pulses. The RESOLUTION control is used to specify the value of the least significant digit (100 ns-10 ms). Use the following procedure when making period measurements:

1. Set the front panel controls as follows:

   FUNCTION - PER A
   RESOLUTION - as required, or AUTO
   SEP/COM - SEP
   ATTENUATION - fully clockwise, X10

2. Connect the signal to be measured to the CHANNEL A input connector.

3. Adjust the variable attenuation control (Channel A) counterclockwise until a stable display is seen. If this cannot be accomplished in the X10 range, return the variable control fully clockwise and change the range to X1. Now again reduce the variable attenuation (counterclockwise) until a stable display is seen.

2-110. Period Averaging Measurements (PER AVG A)

2-111. Multiple periods of frequencies between 5 Hz and 1 MHz may be averaged to obtain even greater resolution and accuracy than with Period measurements. The RESOLUTION control now uses the 10^0-10^5 range to define the number of periods averaged. For example, with a Period measurement of a 1 kHz signal, the display would read "1.0000 ms"; the resolution of the Least Significant Digit is 100 ns. In Period Averaging, the same signal would be maximized at a display of "1000.000 μs" the resolution has increased to 1 ns. The number of periods measured, N, is selected in consecutive powers-of-ten. The total clock pulse count for all periods measured, is accumulated; the decimal point is then shifted for averaging. Resolutions vary from 100 ns to 1 ps. As N increases, the average value approaches the correct value. For N periods, the accuracy is:

$$\frac{100 \text{ ns} \pm \text{Trigger error} \pm \text{time base error}}{N}$$

Use the following procedure when making period averaging measurements:

1. Set the front panel controls as follows:

   FUNCTION - PER AVG A
   RESOLUTION - as desired, or AUTO
   SEP/COM - SEP
   ATTENUATION - fully clockwise, X10

2. Connect the signal to be measured to the CHANNEL A input connector.

3. Adjust the variable attenuation control (Channel A) counterclockwise until a stable display is seen. If this cannot be accomplished in the X10 range, return the variable control fully clockwise and change the range to X1. Now again reduce the variable attenuation (counterclockwise) until a stable display is seen.

2-112. Time Interval Measurements (T.I. A-B)

2-113. When the instrument makes time interval measurements, the START pulse is generated through Channel A and the STOP pulse is generated through Channel B. Use of the SEP/COM switch can either isolate the Channel A input from the Channel B input or connect Channel A input to both input amplifiers. With the switch in the COM position, events from the same source can be measured by Channel A and Channel B. With the switch in the SEP position, events from two sources can be measured on both channels.

2-114. During time interval measurements, inconsistencies between channels may be noticeable. Hysteresis (sensitivity) levels will not be precisely the same for both Signal Conditioners. Depending on ATTENUATION control settings, triggering at different levels of the input signal may also be a problem between channels. It is therefore suggested the the operator monitor the input signals with an oscilloscope.

2-115. There are several important specifications regarding the input signals for time interval measurements. The minimum time between the start level on Channel A and the stop level of Channel B can not be less than 100 ns (the maximum display resolution). Times less than 100 ns will cause the 7250A to gate (GATE LED on), but the display will read zero. The pulse width for either start or stop signal should be at least 250 ns. The time between the stop of one interval measurement and the start of the next is determined by the instrument's cycle rate (250 ms).

2-116. Triggering problems may appear in a number of ways when measuring time interval. An illuminated, but not flashing, GATE LED could mean that a proper stop signal is not being applied to Channel B. If the GATE LED is flashing, but there is no display, one or both of the input frequencies may be too high. Keep in mind that the 7250A is limited to a maximum of 2 MHz in Time Interval mode. Ringing on the input signal may be lessened by increasing the ATTENUATION or by using an appropriate termination.

NOTE

The time interval function should not be used when period measurements are to be made.

2-117. Use the following procedure when making time interval measurements:

1. Set front panel controls as follows:

   FUNCTION - T.I. A-B
   RESOLUTION - as desired, or AUTO
   SEP/COM - SEP if the start and stop signals are from separate sources. COM if the start and stop signals are from the same source.
   OFFSET CONTROL - ∿ (both channels)

CHANNEL A SLOPE - set to + for triggering on the positive slope of the input, or to – for the negative slope.
CHANNEL A ATTENUATION - set variable and X1 X10 controls for maximum attenuation (CW, X10).
CHANNEL B SLOPE - + or – as required
CHANNEL B ATTENUATION - set to maximum (CW, X10)

2. For separate input signals, connect the start signal to CHANNEL A input connector and the stop signal to CHANNEL B. For common inputs, connect the signal to Channel A.

3. Adjust variable attenuation control (CHANNEL A) counterclockwise until the GATE LED comes on. If this cannot be accomplished in the X10 range, return the variable control fully clockwise and change the range to X1. Now again reduce the variable attenuation (counterclockwise) and look for a GATE LED indication.

4. Decrease attenuation on the CHANNEL B input in a similar manner until the GATE LED begins to flash, ensuring proper stop triggering.

NOTE

If COM is selected, the Channel A X1 X10 ATTENUATION control affects both channels and the Channel B X1 X10 control is disabled.

2-118. Totalizing Measurements (TOT A)

2-119. In the totalize mode, the 7250A can be used to continuously count and display the number of events occurring on Channel A. Only a reset will reinitialize the count. Use the following procedure for totalize measurements:

1. Set front panel controls as follows:

FUNCTION - TOT A
RESOLUTION - not used
SEP/COM - SEP
ATTENUATION - fully clockwise, X10

2. Connect signal to be totalized to CHANNEL A input connector.

3. Adjust the variable attenuation control counterclockwise until a reliable display is seen. If this cannot be accomplished in the X10 range, return the variable control fully clockwise and change the range to X1. Now again reduce the variable attenuation (counterclockwise) until a reliable display is seen.

4. Observe the continuously updating count.

2-120. Self Check (CHK)

2-121. The self check function can be used to verify the digital operation of the 7250A. Each setting of the RESOLUTION control will provide a predictable display of the 10 MHz reference frequency. To self check the 7250A, use the following procedure:

1. Press the power switch to ON.

2. Set the FUNCTION control to CHK.

3. Momentarily press the RESET control; the display should read "8888888".

4. Set the RESOLUTION control to AUTO; the display should read "10000.00 kHz".

5. Verify correct display for each of the remaining six RESOLUTION settings.

Section 3
Theory of Operation

3-1. INTRODUCTION

3-2. The 7250A Universal Counter-Timer will be explained on two levels in this section. FUNCTIONAL DESCRIPTION, referenced to the functional block diagram Figure 3-1, deals with each of the 7250A's more common functions. In addition, each mode of operation will be separately described and illustrated. CIRCUIT DESCRIPTION will then provide a more specific accounting of 7250A operation; various figures present simplified schematic diagrams of these descriptions. Refer to Section 8 of this manual for detailed schematic diagrams and a list of mnemonics.

3-3. FUNCTIONAL DESCRIPTION

3-4. The 7250A Universal Counter-Timer is capable of the following measurements: Frequency (to 80 MHz), Period and Period Average (to 2 MHz), Counts per Minute, Time Interval, Ratio, Totalize, and Self Check. The instrument employs the functional blocks illustrated in Figure 3-1. Each block performs the following operations:

1. Control Logic: This block provides logic and timing functions for the 7250A. RESOLUTION and FUNCTION settings are decoded and appropriate decimal point placement and measurement units annunciators supplied to the Display. Control Logic produces six resolution dependent, decade divided frequencies for control of the Main Gate. Depending on the FUNCTION selected, these frequencies are derived from the Time Base, Channel A input, or Channel B input. Control Logic also supplies autoranging for appropriate functions.

2. Signal Conditioners: These blocks condition the input signal for compatibility with other circuitry within the counter. A Signal Conditioner will provide a pulse train output, with each pulse corresponding to one cycle or event of the input signal.

3. Time Base: Depending on the FUNCTION selected, the Time Base (with dividers) supplies 10 MHz, 1 MHz, 100 kHz, or 1/6 MHz. These four frequencies are supplied by one of the available 10 MHz frequency standards or through the EXT 10 MHz input jack on the 7250A's rear panel.

4. Power Supply: This block utilizes conventional power supply and regulation techniques to supply outputs of +5V to all digital circuitry, -5V to the Signal Conditioners, +12V and -12V to control circuitry. When an optional oven time base is installed, oven voltage (+5V) remains energized when the front panel power switch is placed in STBY.

5. Main Gate: When enabled, the Main Gate passes pulses from the Clock Select functional block to Count and Display. Gate Select (enable) and Clock Select inputs to the Main Gate vary by function, as defined in Table 3-1.

6. Clock Select: This block routes signals to the Main Gate clock input for count and display. The Clock Select block is under direct control of signals from Control Logic.

7. Gate Select: This function enables the Main Gate at a rate determined by Control Logic.

8. Count: The Count function utilizes seven counter decades and latches. An internal oscillator sequences through count, latch, and output periods to provide a BCD output to Display.

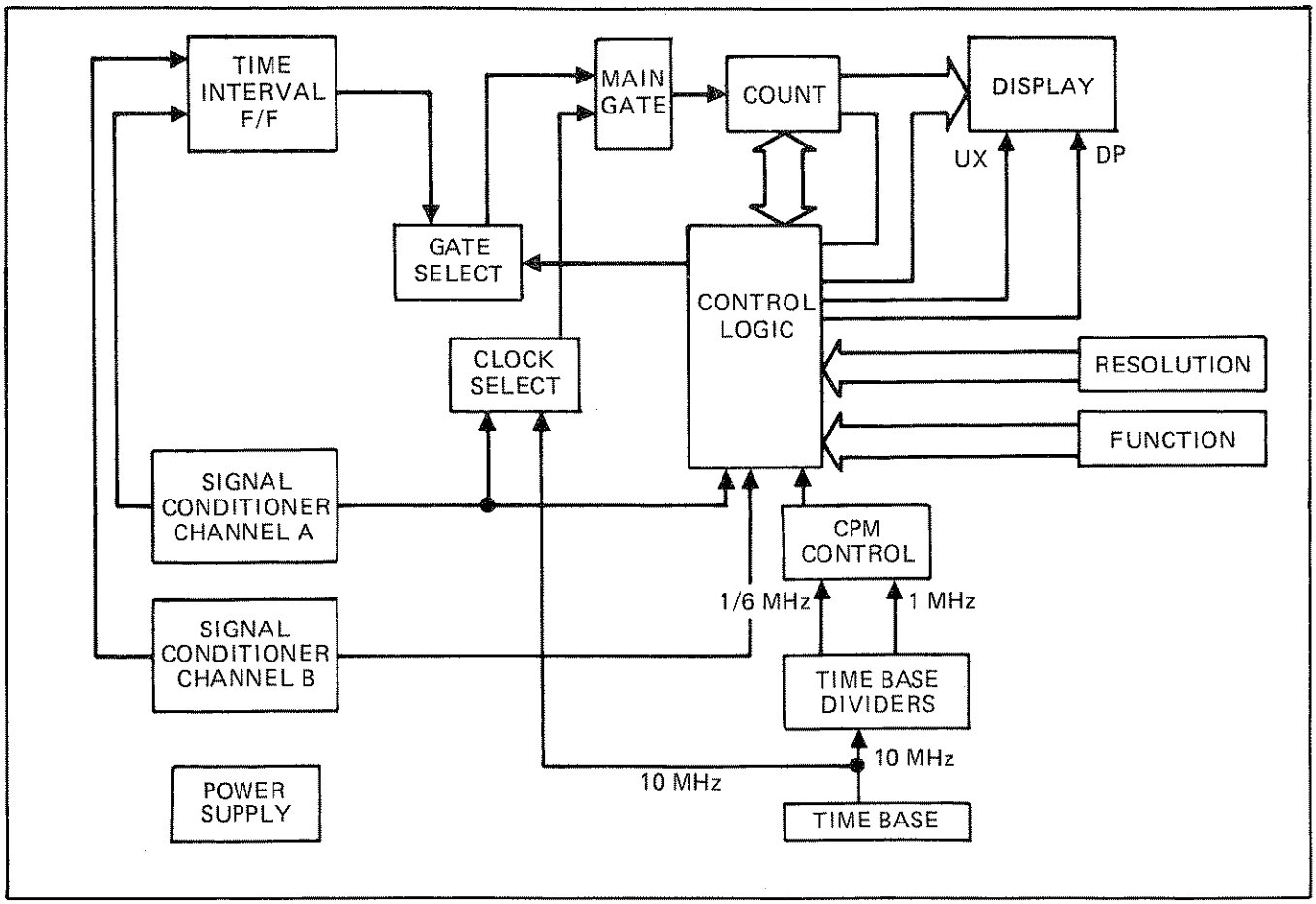


Figure 3-1. 7250A Functional Block Diagram

9. Display: This function provides BCD to seven segment decoding for display of the count. Decimal points and measurement units are determined by Control Logic.

10. Time Interval Flip-Flop: This function derives the start pulse from Channel A and the stop pulse from Channel B for enabling of the Main Gate.

11. CPM Control: When in the Counts per Minute function, this functional block overrides RESOLUTION settings and routes the 1/6 MHz Time Base to Control Logic; a fixed gate time of 600 ms is established. In addition, this block disables decimal point and measurement unit outputs to the Display.

3-5. Frequency (FREQ A) Measurements

3-6. When used in this mode, the 7250A will accumulate and display cycles of an input frequency for a specified length of time. This interval, known as the gate time, may be 0.1 ms, 1 ms, 10 ms, 0.1s, 1.0s, or 10s. The positioning of the decimal point, as determined by the range setting, will translate the displayed cycle count to units of kHz or MHz. For example, an input frequency of 2.3 MHz being measured on the 100 Hz RESOLUTION setting would yield a display of (x x 2 . 3 0 0 0 MHz). The gate time, in this case 10 ms, would allow 23,000 cycles of the input frequency to be counted; the displayed number without decimal point will always equal the actual number of cycles counted during the gate time. This count would then be displayed as the input frequency by repositioning of the decimal point and illumination of the MHz units annunciator.

3-7. Frequency (FREQ A) mode is illustrated on an operational function level in Figure 3-2. Control Logic determines most other function operation. In particular, the 1 MHz reference is decade divided by Control Logic to provide the six gate times for Gate Select. Clock Select is set by Control Logic signals to route the Channel A input to the Main Gate. With the Main Gate enabled by Gate Select, the Channel A frequency will be transferred to Count and Display.

3-8. Period (PER A) Measurements

3-9. The period of the Channel A input signal is measured by counting a reference frequency for an interval determined by the input signal. Depending on the RESOLUTION setting, the 7250A will count a reference

Table 3-1. Main Gate Inputs

FUNCTION	CLOCK SOURCE	GATE SOURCE
FREQ A	Channel A Input	Decaded Time Base from Control Logic.
CPM X100A	Channel A Input	600 msec from Control Logic
RATIO A/B	Channel A Input	Channel B Input
PER A	Decaded Time Base from Control Logic	Channel A Input divided by Control Logic
PER AVG A	10 MHz Time Base	Channel A Input divided by Control Logic
TI A – B	Decaded Time Base from Control Logic	Determined by Channels A and B Inputs
TOT A	Channel A Input	Constant Enable from Control Logic
CHK	10 MHz Time Base	Decade divided 10 MHz Ref

frequency of 10 MHz, 1 MHz, 100 kHz, 10 kHz, 1 kHz or 100 Hz. The display will then show the total count of the reference frequency for the period of one cycle of the input frequency. With repositioning of the decimal point and illumination of the "msec" or "sec" units annunciator, this count will identify the period of one Channel A input cycle. For example, with a Channel A input frequency of 400 kHz set for PER A measurement with 100 ns RESOLUTION, the 7250A will count a 10 MHz reference frequency for 2.5 μs. A count of 25 will be accumulated and displayed. The RESOLUTION setting will also specify the decimal point and measurement unit for the display; a reading of (x x 0 . 0 0 2 5 ms) will be displayed. The total count of the reference frequency is thereby displayed.

3-10. Period measurement is functionally illustrated in Figure 3-3. Control Logic determines most other function operation. Gate Select will be controlled by the Channel A input frequency, routed through the Control Logic. Clock Select will be derived from the 10 MHz Time Base; either the 10 MHz or one of five decade divided frequencies from the Control Logic will be used to clock the Main Gate. This clock will be fed to Count and Display whenever the Main Gate is enabled by Gate Select.

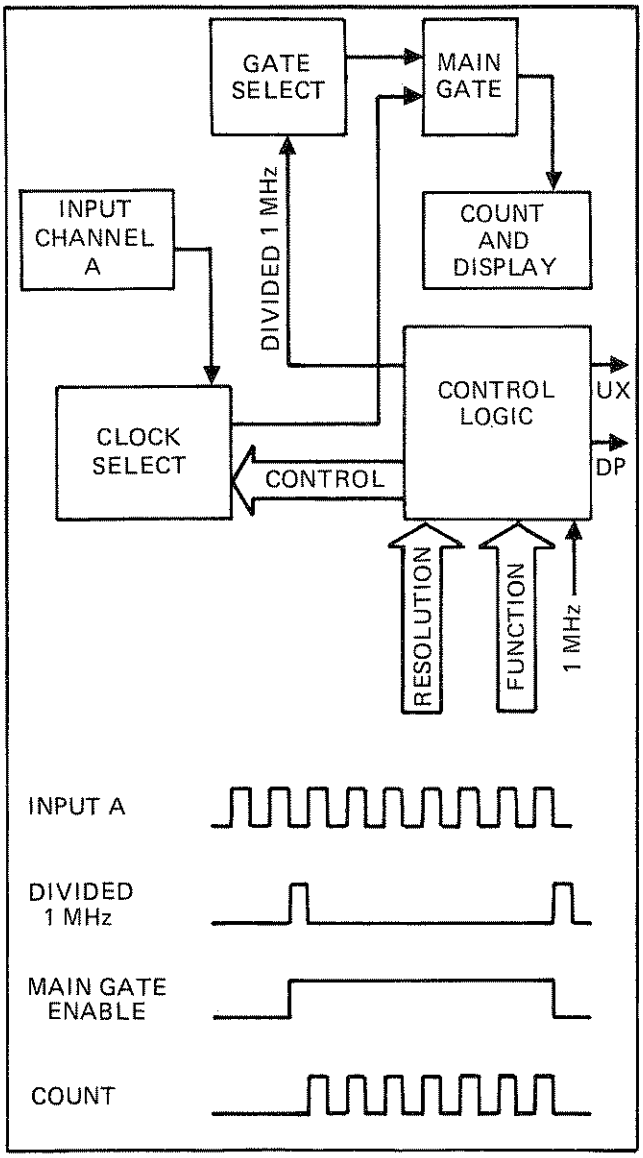


Figure 3-2. Frequency Measurement

3-11. Period Averaging (PER AVG A) Measurement

3-12. During period averaging measurements, the 7250A will count a reference frequency for an interval equal to multiple cycles of the Channel A input frequency. The Front Panel RESOLUTION control will determine the number of input cycles during which the reference frequency is counted (10^0 - 10^5 input cycles in decade steps). The reference frequency will now be the instrument's 10 MHz time base only. As in period measurements, the decimal point and units annunciator will be utilized to display the average elapsed time for one period of the Channel A input frequency. As an example, a 400 kHz Channel A input signal could be measured with the RESOLUTION control set to "10^3". The 10 MHz reference frequency will now be counted for 1000 cycles of the input signal: 25,000 counts will be displayed. The

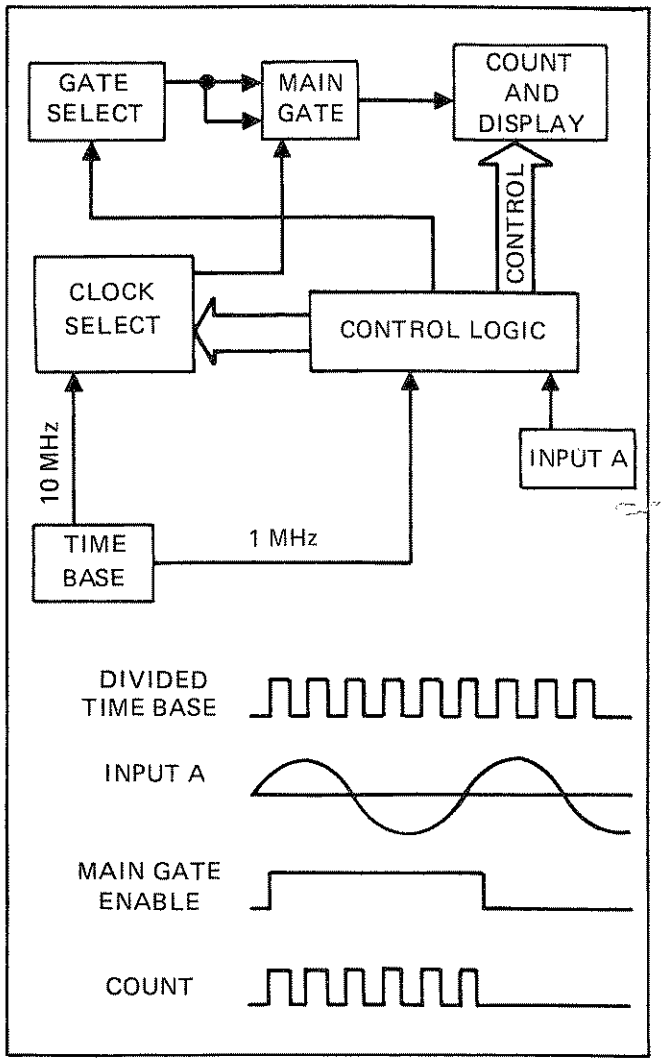


Figure 3-3. Period Measurement

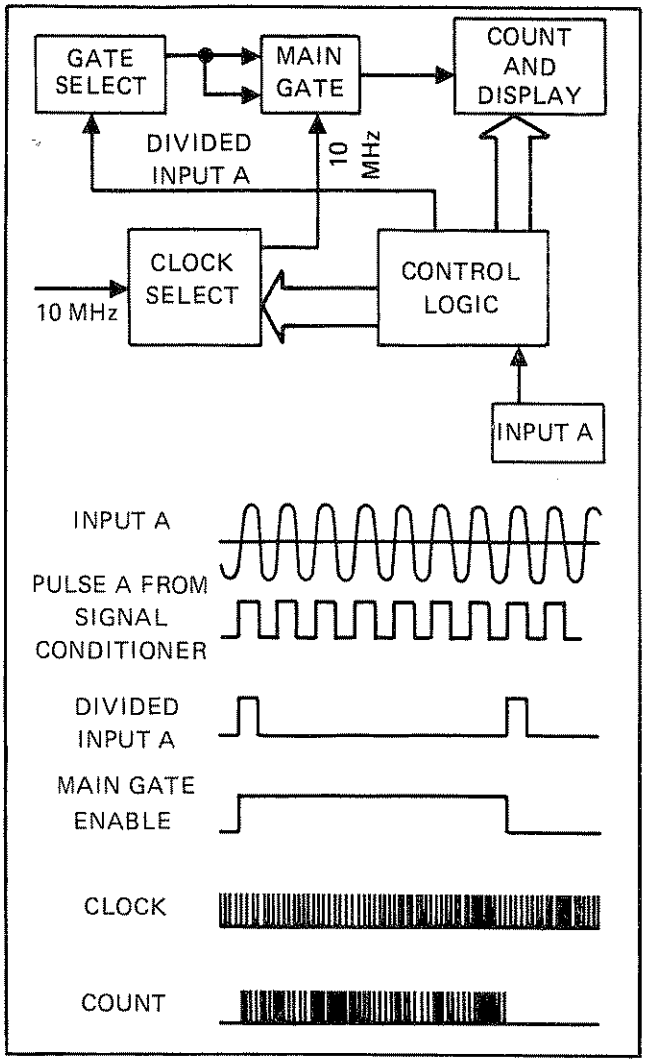


Figure 3-4. Period Average Measurement

decimal point and units annunciator will specify the display to read (x x 2 . 5 0 0 0 μs). The display's resolution is thereby greatly enhanced. A resolution of 100 ps is shown in Period Average, whereas the same signal exhibited only 100 ns resolution in the Period measurement example.

3-13. An illustrated functional approach to Period Average measurement is provided in Figure 3-4. Program Control Logic enables Clock Select to apply the 10 MHz time base to the Main Gate. The input frequency (Input A) is decade divided by Program Control Logic; depending on the RESOLUTION setting, the Channel A frequency or one of five derived frequencies is applied to Gate Select. The Main Gate is thereby enabled for an interval equal to 10^0 to 10^5 cycles of the Channel A input. When enabled, the Main Gate feeds the 10 MHz reference to Count and Display. Program Control Logic then determines display update, decimal point placement and units annunciation.

3-14. Counts per Minute (CPM X100A) Measurement

3-15. The 7250A will display revolutions per minute (RPM) when used in this mode. A 100 count per revolution transducer must be used as the input to Channel A. The front panel RESOLUTION control will have no effect in this mode; the instrument will display a fixed resolution of 100 CPM. Each count will progress for 0.6s. There will be no decimal point or units annunciator activated.

3-16. Counts per Minute measurement is shown on a functional level in Figure 3-5. Time Base Dividers provide a 1/6 MHz reference frequency to CPM Logic. CPM Logic performs three functions. First, the 1/6 MHz reference is routed to Program Control Logic. Secondly, CPM Logic provides a fixed range setting. Finally, decimal point placement and units annunciators are disabled. Program Control Logic decade divides the 1/6 MHz reference to 1 2/3 Hz: Gate Select thereby enables

the Main Gate for 0.6s. Clock Select routes the input on Channel A to the Main Gate to be fed to Count and Display.

3-17. Ratio (RATIO A/B)

3-18. Ratio measurement yields a numeric display, without measurement units, of the Channel A signal (5 Hz-80 MHz) divided by the Channel B signal (5 Hz-1 MHz). Refer to Figure 3-6 for the following block description. The Channel A input, always the higher frequency, is routed to the Main Gate through Clock Select. The Channel B input is decade divided within Control Logic. Depending on the RESOLUTION setting, one of six derived frequencies then enables the Main Gate through Gate Select. The number of pulses of the Channel A Signal counted during the main gate enable is then displayed without measurement unit. This displayed number is the cycle count of the Channel A signal during one period of the divided Channel B signal. With decimal point placement, this number yields the ratio between the two inputs. For example, with 5 MHz on Channel A, 500 kHz on Channel B and a RESOLUTION setting of 10^1, the Main Gate will be enabled for 20 μs. During this time, 100 cycles of the Channel A frequency will be counted, and the display will yield a reading of "10.0".

3-19. Totalize (TOT A)

3-20. During totalize measurements, the number displayed represents a continuing total number of

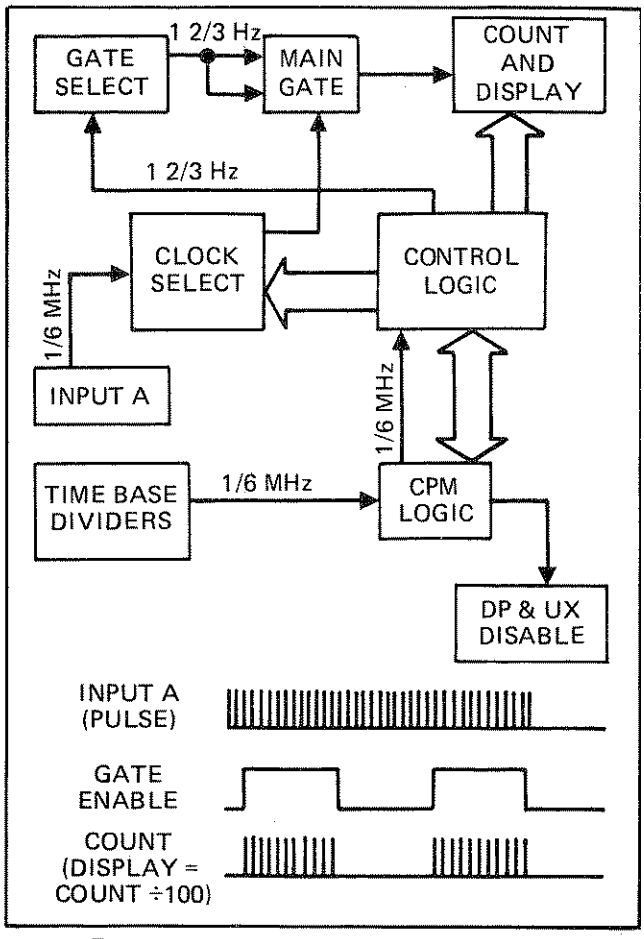


Figure 3-5. Counts Per Minute Measurement

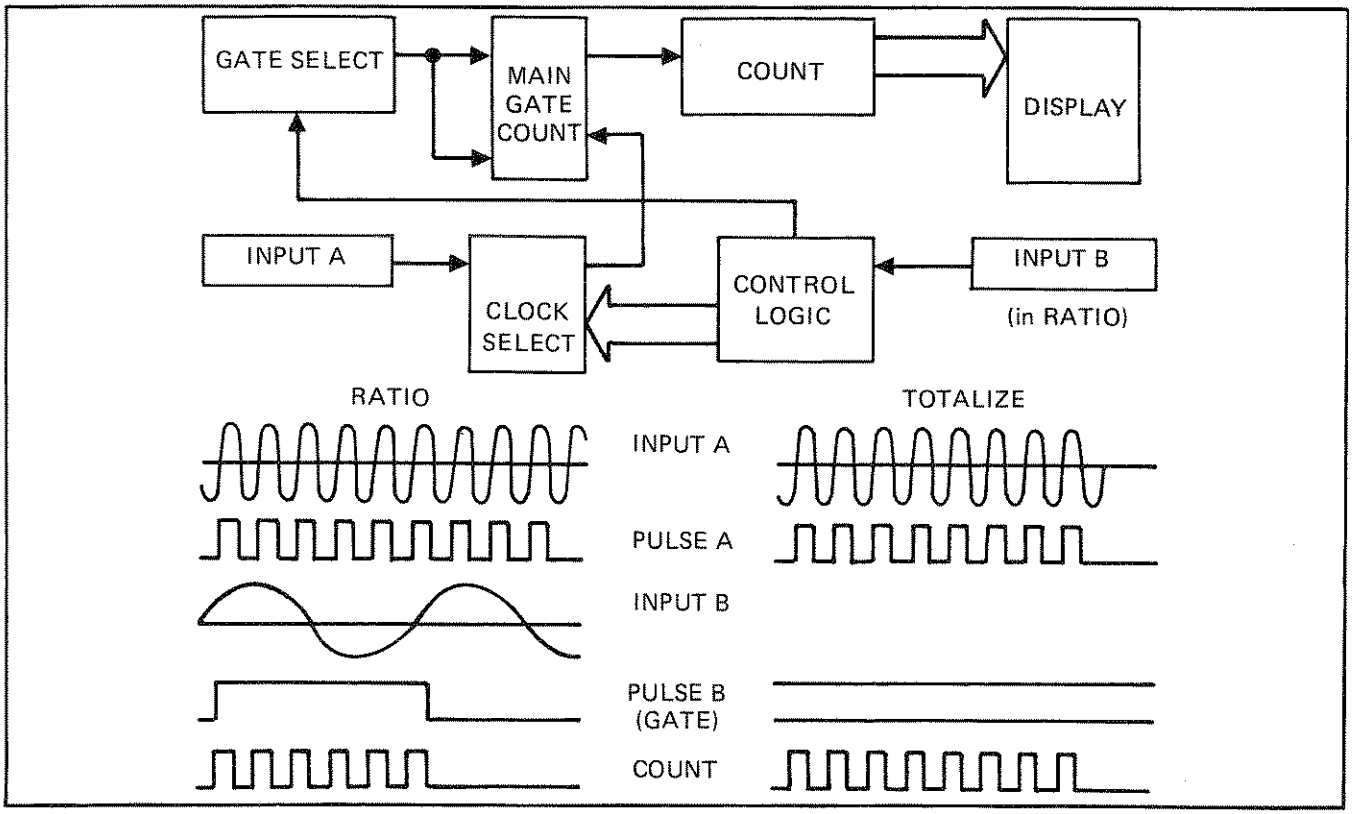


Figure 3-6. Ratio and TOT A Block Diagram

triggering events that occur on Channel A. The 7250A will restart this count only when a reset is applied. No measurement units or decimal points are used during totalize measurements. Refer to Figure 3-6 for the following functional block description. A constant Main Gate Enable is supplied from Control Logic through Gate Select. Channel A input pulses clock the Main Gate and are displayed to a maximum count of "9999999".

3-21. Time Interval (T.I. A-B)

3-22. For time interval measurements, the 7250A will display counts of a scaled reference frequency for a period whose start is determined by the Channel A input signal and whose stop is determined by the Channel B signal. Refer to Figure 3-7 during the following block diagram discussion. One of six reference frequencies is selected by the RESOLUTION Control for routing through Clock Select to the Main Gate. These frequencies are the 10 MHz time base and five derived frequencies (1 MHz-100 Hz) from Control Logic. Gate Select is held enabled by Control Logic, allowing the Time Interval Flip-Flop to control Main Gate enabling. Depending on the Slope Control setting, a positive or negative going Channel A input will now enable the Main Gate to pass the reference frequency. Under similar control, the Channel B signal will disable the Main Gate. The accumulated counts of the reference frequency between A and B inputs are displayed as in Period measurements.

3-23. Self Check

3-24. In the self check mode, the 10 MHz reference frequency is used as a dynamic verification of counter digital circuitry operation. Input and signal conditioning circuitry cannot be checked in this mode. Each setting of the RESOLUTION control yields a predetermined display readout as defined in Table 3-2. Refer to Figure 3-8 during the following block description. Control Logic disables inputs from the Channel A Signal Conditioner while providing standard digital control for Clock Select, Gate Select, Count and Display functional blocks. Clock Select routes 10 MHz from the Time Base to the Main Gate. Depending on the RESOLUTION setting, Gate Select enables the Main Gate for a duration derived from the 10 MHz reference in Control Logic. The 10 MHz Clock Select frequency is thus counted and displayed for gate times of 0.1 ms to 10s. Overflow indication will occur at the 1 Hz and 0.1 Hz settings.

3-25. CIRCUIT ANALYSIS

3-26. The following descriptions detail key circuit operation in the 7250A. Circuit descriptions for options are presented in Section 6 of this manual. It is recommended that the FUNCTIONAL DESCRIPTION be read first for an overall understanding of the

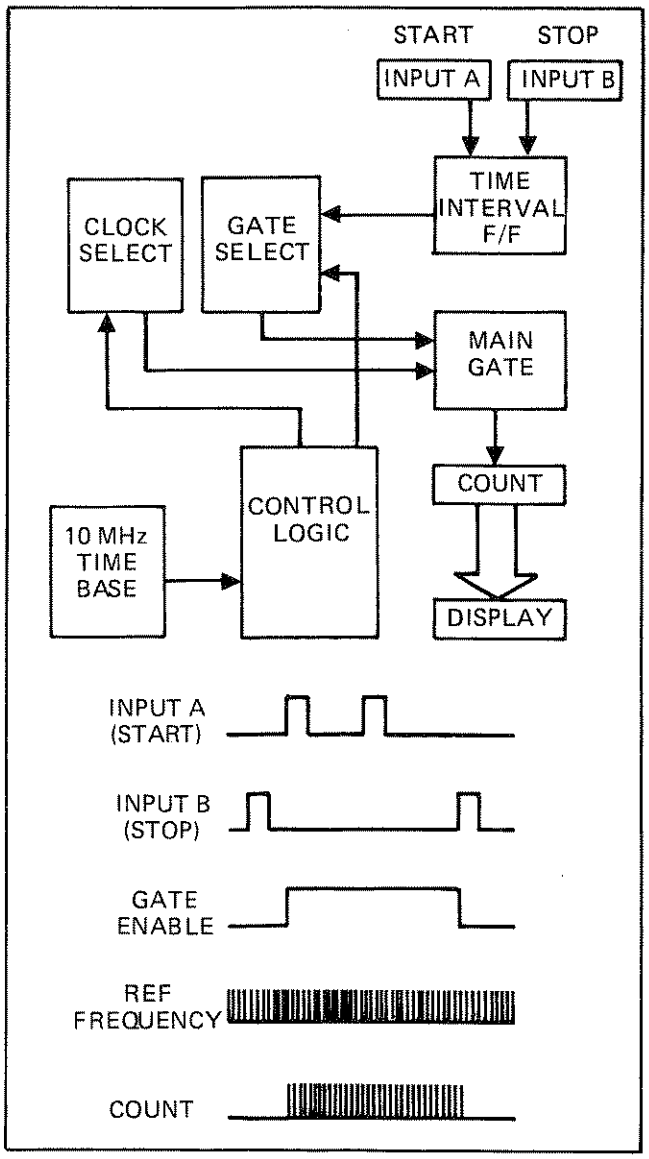


Figure 3-7. Time Interval Block Diagram

instrument. The simplified schematic diagrams presented here are referenced in the applicable paragraphs. Complete schematic diagrams and mnemonic definitions will be found in Section 8.

3-27. Power Supply

3-28. The 7250A Power Supply utilizes standard ac to dc rectifying, filtering and regulating circuitry to provide regulated outputs of -5V, +5V, -12V, and +12V. Accomodation to line voltages of 100V, 120V, 220V or 240V is achieved through positioning of S4 and S5 in the power transformer's primary. The -5V (reg) is supplied by tracking regulator U25. The Front Panel ON/STBY switch (S3) disconnects the regulated voltages from 7250A circuitry; the STBY position will maintain +5V to any installed oven option.

Table 3-2. Display Readout in Self Check Mode

RESOLUTION	DIGIT DISPLAY	MEASUREMENT UNIT
10 kHz	XXX10.00	MHz
1 kHz	XX10.000	MHz
100 Hz	X10.0000	MHz
10 Hz	10000.00	kHz
1 Hz	0000.000	kHz (OVFL)
0.1 Hz	000.0000	kHz (OVFL)
AUTO	10000.00	kHz

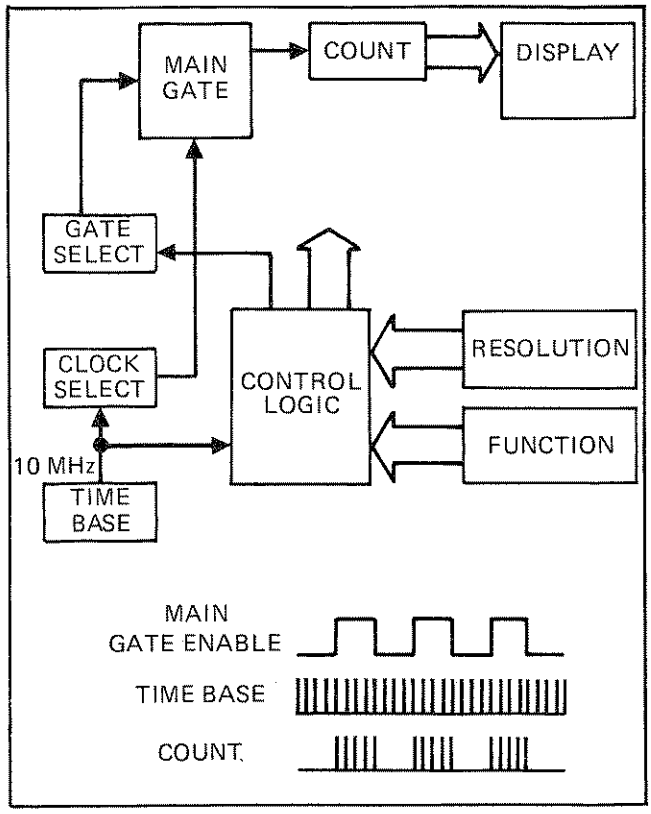


Figure 3-8. Self Check Functional Block Diagram

3-29. Time Base

3-30. The 10 MHz reference is supplied by an internal free-air time base, an optional internal time base, or by an external time base applied through the rear panel connector. Schmitt Trigger U19-2 provides a 10 MHz TTL output from whichever time base is utilized. This reference is decade divided by counter U20-13, providing a 1 MHz signal to Control Logic input CI (U13-12). This reference is passed by selector U6-6 whenever CPM mode is not selected. The 1 MHz signal from U20-13 is also decade divided by U20-3 to provide 100 kHz for the gate synchronizer U28-8. Divide-by-six counter U12-8 uses the 1 MHz signal to derive a 1/6 MHz reference to be used for CPM measurements. Further decade division of the 1 MHz or 1/6 MHz (in CPM) reference occurs within Control Logic. The rear panel EXT-INT switch must be placed to EXT when an external time base is applied through the rear panel connector. With the switch in EXT, power is removed from the internal time base; if an oven option is installed, the oven will cool.

3-31. Input Circuitry

3-32. Identical input circuitry is utilized for Channel A and Channel B. For either Channel, the input signal is amplified, filtered, and shaped to provide an output at ECL logic levels. Figure 3-9 illustrates input circuitry for either channel. Each input is fuse protected (250 mA) and is ac coupled to the appropriate X1 X10 ATTENUATION control. In the X1 position, each input is applied directly to the Signal Conditioner; in the X10 position, each input is first applied through the attenuation network in the Signal Conditioner.

3-33. Within the Signal Conditioner, the signal passes two clamping diodes and an input buffer prior to entering the Preamplifier IC. The preamplifier contains an amplifier, a Schmitt Trigger for signal shaping, and an ECL driver. Offset controls R34 (for Channel A) and R26 (for Channel B) can be adjusted to optimum triggering levels. In addition, the Trigger Offset control provides front panel controlled trigger level offset voltages of −150 mV, 0, and +150 mV. The variable ATTENUATION control is used to adjust the Input Amplifier gain. This control, when used in conjunction with the X1 X10 control, provides attenuation ranges of 1-10 (X1) or 10-100 (X10). Hysteresis resistors R32 (for Channel A) and R35 (for Channel B), located on the Main PCB, set hysteresis window levels for the Schmitt Trigger. The FILTER can be used to vary the Input Amplifier bandwidth to attenuate signals above 100 kHz.

3-34. Function Logic

3-35. The levels on function lines F1, F2, F4, and F8, as determined by the setting of FUNCTION switch S2, control the routing of Clock Select, Gate Select, and Time Base signals. Lines F1, F2, and F4 are decoded by Control Logic U13; see Table 3-3 for function line coding. Each change of the FUNCTION switch setting will also cause an instrument reset when decoded. The Clock Select output (Channel A input, 10 MHz reference, or CO from Control Logic) is determined by outputs EA and EH from Control Logic. The Gate Select output is determined by the clocking of the Main Gate Flip-Flop at GC (U13-40). These outputs are further defined in Table 3-4.

3-36. When Counts per Minute (CPM X100A) is selected, F8 is high and U14-13 is enabled. With F4 low, U14-11 goes high to enable U6-5. The CI input to Control

Logic thereby switches from 1 MHz to 1/6 MHz. The U14-11 high also disables Resolution Multiplexer U21, decimal point driver Q4, and measurement unit driver Q5. The display in CPM is thus set for one resolution and no decimal point or measurement unit annunciation. Finally, with the same F1, F2, and F4 code as FREQ A, the decoded CPM logic (U14-11) also disables the gate synchronizer via U29-9.

3-37. Resolution Logic

3-38. The front panel RESOLUTION switch sets logic levels on line R1, R2 and R4. These levels are decoded within Control Logic to enable the output from one of six decade dividers; a gate time ranging from 0.1 ms through 10s is thus provided. Each change of the RESOLUTION control also generates a range reset using the reset multivibrator (U1-12).

3-39. During autoranging, Control Logic will sequence through the available resolutions for the function in use. The sequence will stop when the Most Significant Digit (MSD) is filled or when the maximum gate time allowed has been reached. Autoranging is disabled in CPM and

Table 3-3. Function Coding

F1	F2	F4	F8	
0	0	0	0	Frequency A
1	0	0	0	Ratio A/B
0	1	0	0	Period A
1	1	0	0	Period Average A
0	0	1	0	Time Interval A to B
1	0	1	1	Totalize A
0	0	0	1	CPM
1	1	1	0	Self Check

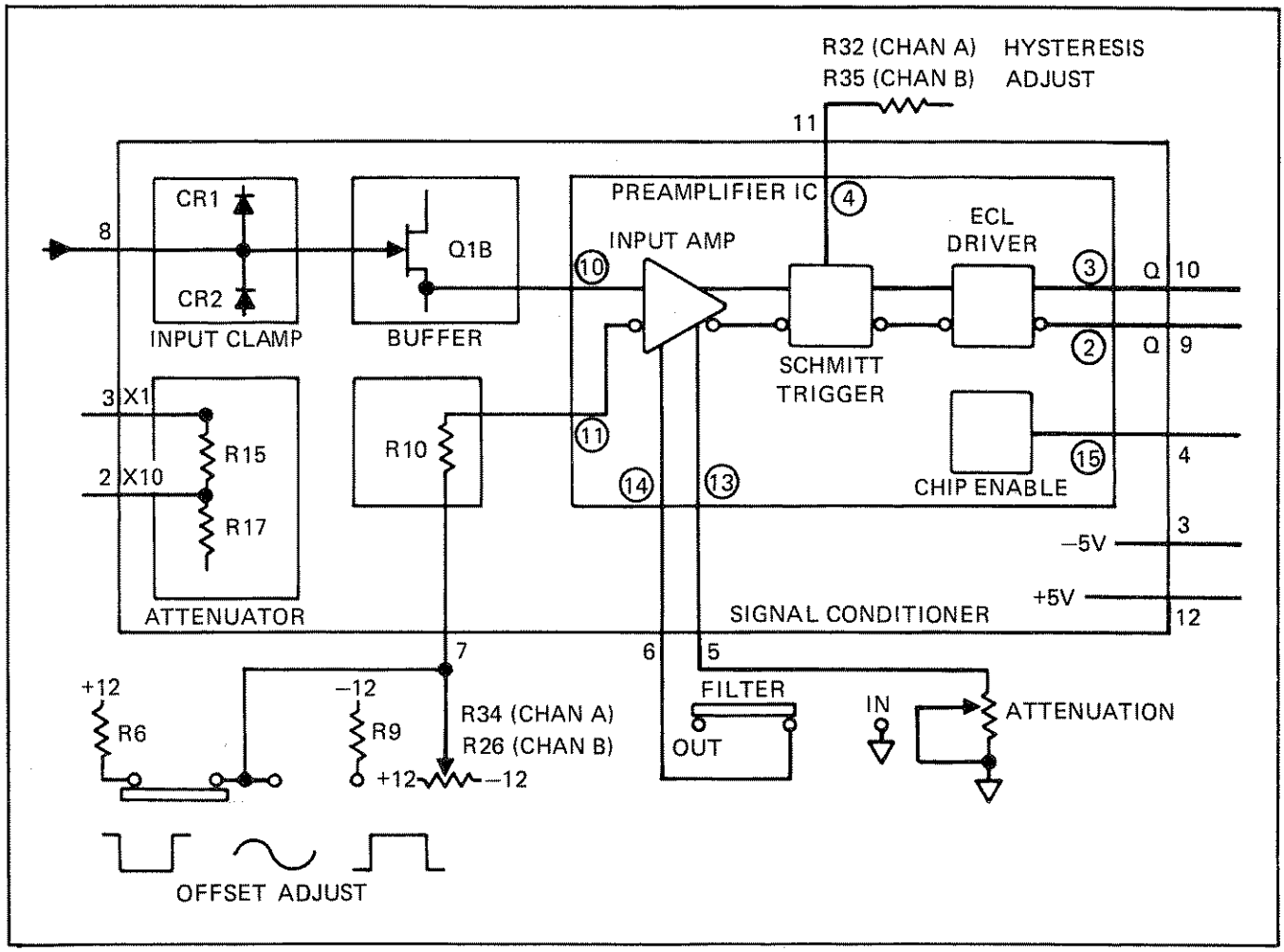


Figure 3-9. Input Circuits Simplified Schematic

Table 3-4. Control Logic Decade Inputs, Outputs

FUNCTION	INPUT DESCRIPTION	OUTPUT DESCRIPTION
FREQ A	10 kHz derived from input of 1 MHz at CI	10 kHz to 0.1 Hz in 6 decade steps at GC
CPM	1/6 MHz at CI	1 2/3 Hz at GC
RATIO A/B	Channel B input (5 Hz → 1 MHz)	1 of 6 decades at GC
PER A	1 MHz at CI	1 MHz to 10 Hz in 6 decade steps at GC
PER AVG A	Channel A input (5 Hz → 1 MHz)	1 of 6 decades at CO
TI A-B	1 MHz at CI	1 MHz to 10 Hz in 6 decade steps at CO
TOT A	Not used	High at GC
CHK	10 kHz derived from input of 1 MHz at CI	10 kHz to 0.1 Hz in 6 decade steps at GC

TOT A modes. Measurement unit annunciators and decimal points will not be changed during autoranging. An iteration counter within Control Logic will step through the allowed resolution settings. A measurement sequence is initiated for each step; if, at the end of a sequence, the counter is not set to the maximum allowable resolution step, either a new measurement sequence is begun at the next higher resolution or the display is updated.

3-40. When the reading is only marginally best resolved in one setting, or is varying slightly, an unnecessary shift in resolution will be prevented by a hysteresis circuit in Control Logic (U13). The hysteresis flip-flop becomes activated when the MSD reaches 1; the resolution will be held until the Second Significant Digit (2SD) falls below 8. The circuit thereby allows input frequency changes of up to 20% to occur without resolution change.

3-41. Control Logic

3-42. The Control Logic integrated circuit (U13) provides most logic and timing requirements for the 7250A. With the exception of Counts per Minute mode, Control Logic performs all FUNCTION decoding. RESOLUTION settings are also decoded to provide the proper decoding and decimal point placement. Together, FUNCTION and RESOLUTION decoding provide proper measurement unit annunciation. In the following paragraphs, general Control Logic operations inputs and outputs will be discussed. A brief description of pin designations is presented in Table 3-5.

3-43. Control Logic provides six decade counters for time base division. Inputs and outputs for the counters are defined by function in Table 3-4. Outputs at pin GC will, by clocking the Main Gate Flip-Flop, enable the Main Gate. Outputs at pin CO will clock the Main Gate. Control Logic will also provide certain gating control signals. Refer to "Main Gate Clocking Logic" and "Main Gate Enabling Logic" for descriptions.

3-44. A general reset ($\overline{R}$) is sourced by Control Logic whenever a new function is decoded. Inputs at RI (U13-7) from the front panel RESET switch, the reset one-shot (U1-12), or the remote interface will also cause a general reset. An $\overline{R}$ signal will reset the seven display decade counters, along with the overflow flip-flop in the Counter Multiplexer U15; the display is set to zero, and a new measurement sequence is initiated. The remote start signal (ST) differs in that the display is not set to zero, while a new measurement sequence is still begun. The decimal point (DP) output is controlled by the decoded RESOLUTION setting and by the strobe inputs from counter-multiplexer U15. The measurement cycle rate (time between successive measurements) is determined by an exterior RC network connected to pin CR. In the 7250A, this cycle time is set at 250 ms. The 7250A will normally start a new measurement cycle automatically. The input on pin SC will allow Control Logic to stop after one measurement. This feature is controlled by a remote start/stop command.

3-45. When set for autoranging, Control Logic utilizes two feedback paths to the Counter-Multiplexer U15-AO and AR. An internal iteration counter will step through the available resolutions until a Carry 6 is seen on AR or until the lowest resolution step has been reached. Autoranging is not available in TOT A or CPM X100A. An internal hysteresis flip-flop is connected to line AO to prevent needless resolution changes during marginal or slightly varying inputs. An internal 14 stage static shift register controls sequencing during the measurement cycle.

Table 3-5. Control Logic Pin Designations

PIN	MNEMONIC	DESCRIPTION	PIN	MNEMONIC	DESCRIPTION
1	Vss	+5V, +/−0.25V	25	EH	Output, enables 10 MHz clock for CHK (all resolutions) and TI A-B or PER (100 ns resolution only)
2	D1	Input, Strobe Line DS2			
3	D2	Input, DS3			
4	D3	Input, DS4			
5	DP	Output, decimal point multiplexed to strobe lines	26	$\overline{GR}$	Output, resets Main Gate Flip-Flop and sets Time Interval start flip-flop
6	UX	Output, units annunciator multiplexed from FUNCTION and RESOLUTION settings	27	$\overline{GS}$	Output, sets Main Gate Flip-F Flop, stays high in CHK and TOT A
7	RI	Input, reset			
8	D4	Input, DS5	28	CO	Output, from decades in PER or TI A-B
9	D5	Input, DS6			
10	D6	Input, DS7	29	Vgg	0V
11	Vdd	−12V, +/−1V	30	ST	Input, start from remote
12	CI	Input, 1 MHz (1/6 MHz in CPM mode)	31	SC	Input, single or continuous counts from remote.
13			32	$\overline{M}$	Output, memory update to Counter-Multiplexer U15
14					
15	XB	Input, from Channel B Signal Conditioner. Used in RATIO A/B	33	BY	Output, Busy (high) when a measurement sequence in process
16	XA	Input, from Channel A Signal Conditioner. Used in PER, PER AVG A.	34	CR	Cycle Rate RC setting
			35	$\overline{R}$	Output, resets decade counters
			36	AR	Input, autorange feedback from Counter-Multiplexer U15
17	EA	Output, LO for TI A-B and CHK.	37	TQ	Input, from time interval stop flip-flop at end of measurement
18	TE	Output, HI for TI A-B.			
19	M1	Inputs, FUNCTION lines from front panel control	38	GQ	Input, from output of Main Gate Flip-Flop
20	M2				
21	M3		39	AO	Input, autorange feedback from overflow flip-flop in Counter-Multiplexer U15
22	R1	Inputs, RESOLUTION lines from front panel control			
23	R2				
24	R3		40	GC	Output, clocks Main Gate Flip-Flop at frequency from 1 MHz through 10 Hz when in TI A-B or PER mode

3-46. Main Gate Clocking Logic

3-47. The Main Gate clock input, as defined by function in Table 3-4, is selected by Control Logic. Figure 3-10 illustrates clocking logic. During FREQ A, CPM and RATIO measurements, control lines EH and CO are held low and EA is high. The Channel A input signal is thereby routed through U30-15 and the ECL-TTL translator (Q1, Q2, Q3) to clock the Main Gate. For Period averaging measurements and the 100 ns setting for T.I. and Period lines EH and CO are high to route the 10 MHz clock signal to the Main Gate. Line EA is held low to disable the Channel A input at U30-11. During time interval measurements, the Main Gate clocking source is derived from the time base divided within Control Logic (U13).

3-48. Main Gate Enable Logic

3-49. The J and K inputs to the Main Gate are function dependent. Referring to Figure 3-11, one of three signal paths may be applied to Gate Selector U6-8. When FREQ A mode is selected, the GQ output from the Main Gate Flip-Flop U5-5 is routed through the Gate Synchronizer U28-8. The synchronizer is clocked by a 100 kHz signal derived from the instrument's time base by decade divider U20-3. Function decoder U29-13 (FA) enables the Gate

Selector to route the synchronized GQ to the Main Gate. In Time Interval mode, GQ is held high and the time interval flip-flops directly control the Gate Selector through U3-6 and U6-8. In all other modes of operation, the GQ output, a decade division of either the Channel A input or the time base, is applied through U6-8 without synchronization. Function decoder U29-1 (FA) enables the Gate Selector to pass this signal.

3-50. The GATE LED annunciator circuits are fed by U3-11 in all function settings. Gate light stretcher U1-13 uses this signal to provide a minimum GATE LED pulse $\overline{(G)}$ of approximately 50 ms. Indication is thus provided of gating in progress, at a discernible rate.

3-51. Count Circuits

3-52. The Main Gate clocking signal is serially applied to seven BCD counters. The four-bit information for Digit 1 is provided by the Main Gate (divide-by-two) and the divide-by-five counter U4. Digit 2 is determined by decade counter U9. The remaining five digits (D3-D7) are derived from the Digit 2 carry within Count-Latch-Multiplexer U15. Figure 3-12 provides a simplified schematic diagram of U15. Digit 1 and Digit 2 are applied to separate 4-bit latches within U15. Digit 2 carry is also applied to the Digit 3 BCD counter. Digits 4-7 are derived from similiar counters and applied to 4-bit latches. Digit

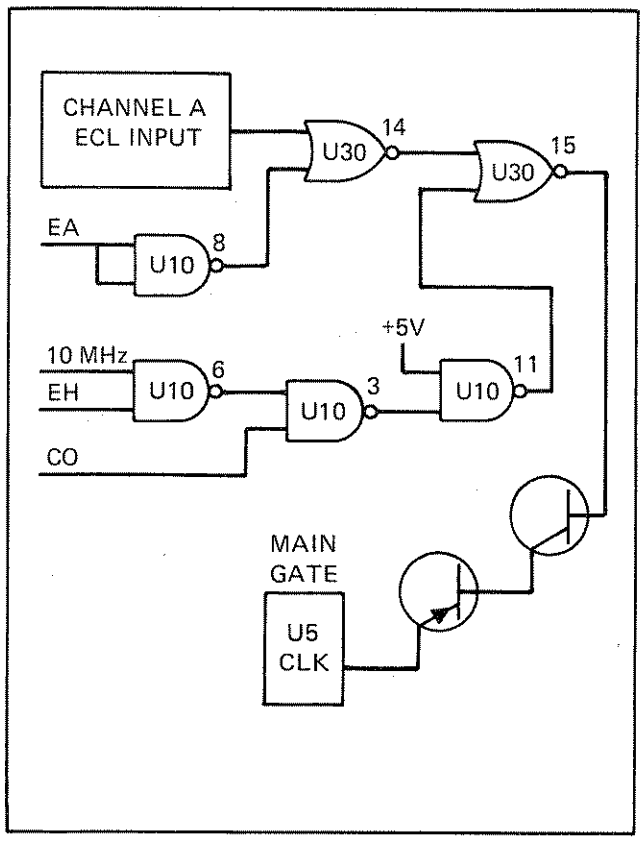


Figure 3-10. Main Gate Clock, Simplified Schematic

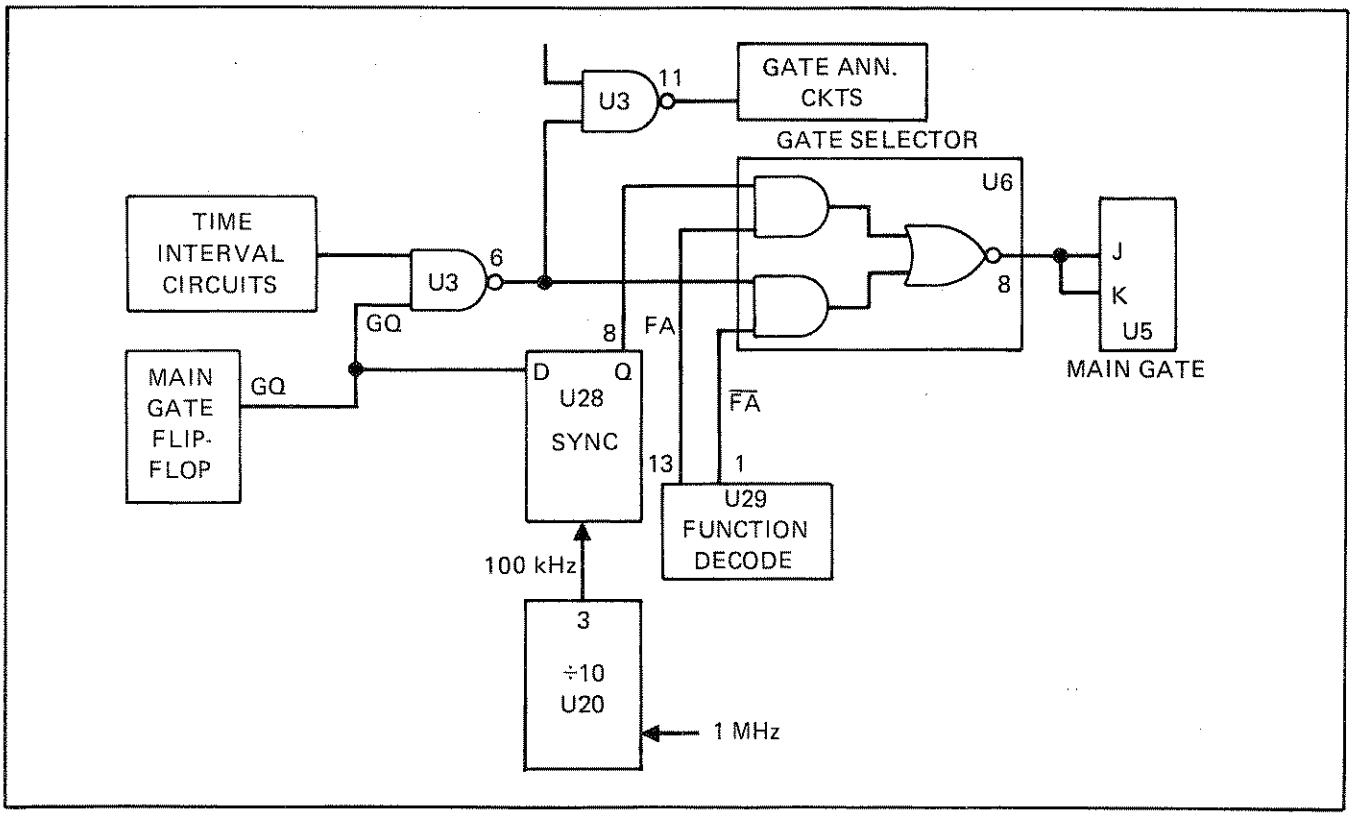


Figure 3-11. Main Gate Enable Logic

1-7 information is loaded into the latches upon receipt of the Memory Update ($\overline{M}$) signal from Control Logic (U13). Any overflow condition (defined as a Carry 7) will be applied to the 1 bit overflow latch at the same time.

3-53. A scan counter within U15 controls latched digit outputs and strobes. This counter is driven by an internal oscillator whose frequency is determined by the exterior connection of C13. As the 4-bit contents of each latch (Digit 1-7) is scanned for output, a simultaneous strobe signal (DS1-DS7) is applied to the appropriate display digit. The contents of all seven latches are thus sequentially displayed. Decimal point placement is provided exterior to U15 by Control Logic (U13).

3-54. Display

3-55. The output from Counter-Multiplexer U15 is applied, through BCD-to-Seven Segment Decoder U22, to all display digits. A strobed output from U15 on lines DS1-DS7 enables the appropriate digit through open collector drivers U16 and U17. In overflow conditions, a latched output is applied directly to the OVFL LED. Control Logic (U13) monitors strobe lines DS2-DS7 to provide decimal point (DP) placement following the correct display digit. Measurement unit (UX) display inputs are supplied by Control Logic function decoding circuits.

3-56. Time Interval Logic

3-57. In the Time Interval function, the Main Gate Flip-Flop (U5-5) is held high, and Main Gate enabling is controlled entirely by two D type flip-flops (U7-8 for interval start, U7-6 for interval stop). Main Gate clocking is provided by the instrument's time base; clocking frequencies from 10 MHz through 100 Hz (respective settings of 100 ns through 10 ms) are selectable with the RESOLUTION control. Control Logic pin EH goes high when 100 ns is selected; the 10 MHz reference is thus fed to the Main Gate. In all other RESOLUTION settings for Time Interval mode, EH is low, and Main Gate clocking is provided from the divided time base at Control Logic pin CO.

3-58. In the initial state, time interval flip-flop U7-10 is set by Control Logic pin $\overline{GR}$ and held clear. Control Logic pin TE is also high, providing the D input for the

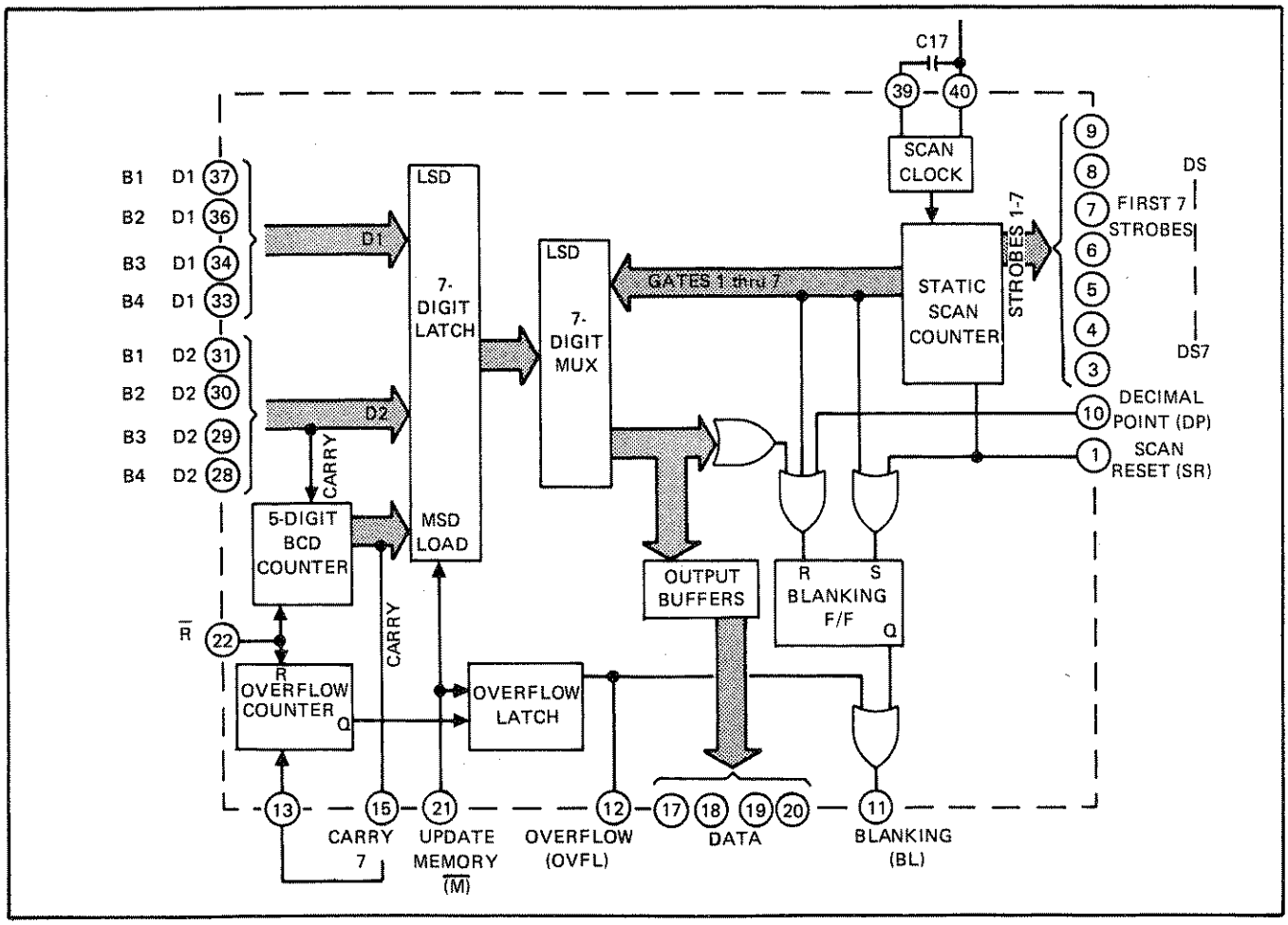


Figure 3-12. Counter, Latches, Multiplexer U15

stop flip-flop and enabling the time interval output gate at U2-13. The Channel A start pulse will now clock U7-11 and enable the Main Gate through U2-6 and U2-11. This same pulse will clear the stop flip-flop. Any subsequent pulse received on Channel B will then clock the stop flip-flop at U7-3, disabling the Main Gate and outputting a pulse to Control Logic pin TQ. Control Logic will respond by waiting 0.1 ms and providing a memory update command ($\overline{M}$).

3-59. Reset Logic

3-60. Reset from Control Logic ($\overline{R}$) clears the decade counters and initializes the display latches. The reset input (RI) to Control Logic is derived in one of four ways. The front panel RESET switch controls RI for as long as it is held depressed. A power on reset will be provided to RI to allow for stabilization of the 7250A's power supply voltages. Monostable multivibrator U1-12 provides time delay and pulse shaping for this reset. A change in the front panel RESOLUTION setting will also cause a pulsed reset from the power on multivibrator. A remote reset will cause the same reset operations as does the RESET switch. Internally, Control Logic (U13) will generate its own $\overline{R}$ whenever a FUNCTION change is decoded. Use of the RESET switch or a remote reset will also place display decoder U22 in lamp test mode; all seven display digits will read "8" for as long as this reset is held applied.

3-61. Remote Logic

3-62. Remote Logic is illustrated in Figure 3-13. When in local operation, remote line $\overline{REM}$ is false, and the SC input to Control Logic is held low by U11-6. The continuous reading mode is thereby enabled. With $\overline{REM}$ false, the ST Control Logic input is also held low by U19-4; Control Logic will therefore not be influenced by conditions on remote lines STR and SCR. When in remote operation, $\overline{REM}$ goes true; SC and ST inputs to Control Logic are no longer held low. Control logic is place in the single reading mode with SC held high by U11-6 and U17-9. Remote line STR is used to trigger each measurement.

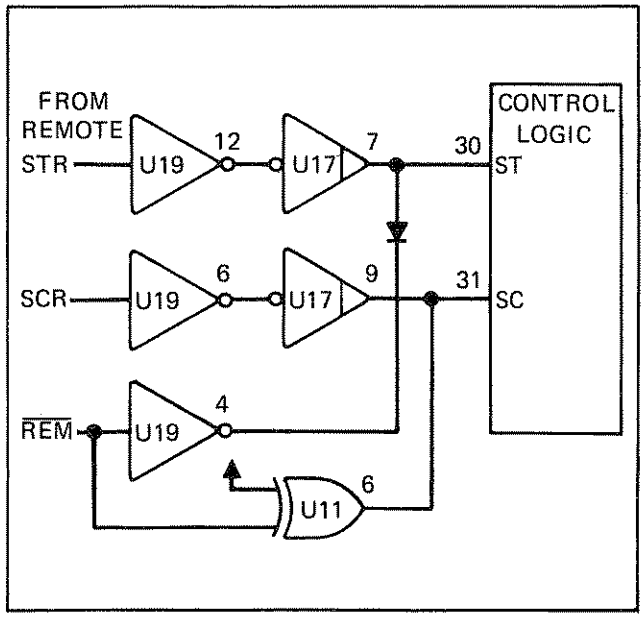


Figure 3-13. Remote Logic

Section 4
Maintenance

WARNING

THESE SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID ELECTRIC SHOCK, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN THE OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO.

4-1. INTRODUCTION

4-2. This section of the manual provides information concerning warranty, general maintenance, performance tests, calibration and troubleshooting for the 7250A Universal Counter-Timer. Test equipment recommended for performance tests, calibration, and troubleshooting is listed in Table 4-1. If the recommended equipment is not available, equipment with equivalent specifications may be used.

4-3. SERVICE INFORMATION

4-4. The instrument is warranted for a period of one year upon delivery to the original purchaser. The WARRANTY is located on the back of the title page of this manual.

4-5. Factory authorized calibration and service for each Fluke product is available at various world-wide locations. A complete list of these service centers is included in Section 7 of this manual. If requested, an estimate will be provided to the customer before any work is begun on instruments that are beyond the warranty period.

4-6. GENERAL MAINTENANCE

4-7. Disassembly

4-8. To disassemble the instrument, use the following procedure:

1. Press the power switch to STBY, and remove the line power cord.

2. On the case bottom, remove the six securing screws. Two of these screws will be found in the middle of the case, under the latches. To access either middle screw, simultaneously pry the two latching rails away from the triangular stop. Pull the latch out far enough to reveal the screws. Refer to Figure 4-1 for an illustrated latch removal procedure.

3. The top half of the case may now be separated from the bottom.

NOTE

Do not hold the case bottom while lifting off the case top. Damage to the Main PCB could otherwise result.

Alternating between front and back panels, pry the case top free of the rest of the instrument. In the front, press down on the BNC input connectors, while gently pulling up on the case top lip. In the rear, press down on the External Reference BNC connector, while pulling up on the top case lip.

4. Remove the single screw at the middle of the Main PCB, and separate the case bottom.

Table 4-1. Required Test Equipment

EQUIPMENT TYPE	REQUIRED BASIC SPECIFICATIONS	WHERE USED	RECOMMENDED TYPE
Oscilloscope	Dual trace (0 - 80 MHz)	Troubleshooting	Tektronix 475
High Frequency Signal Generator	1 - 80 MHz	Calibration Performance Test	Fluke 6160A
Low Frequency Signal Generator	10 Hz - 1 MHz	Calibration Performance Test	Fluke 6011A (equipped with High Performance TCXO)
Digital Multimeter	General Purpose	Troubleshooting	Fluke 8000A
AC RMS Voltmeter	<10 mV rms 5 Hz - 80 MHz	Performance Test	Fluke 8920A Boonton 92-BD
50Ω Adapter		Performance Test	Boonton 91-8B

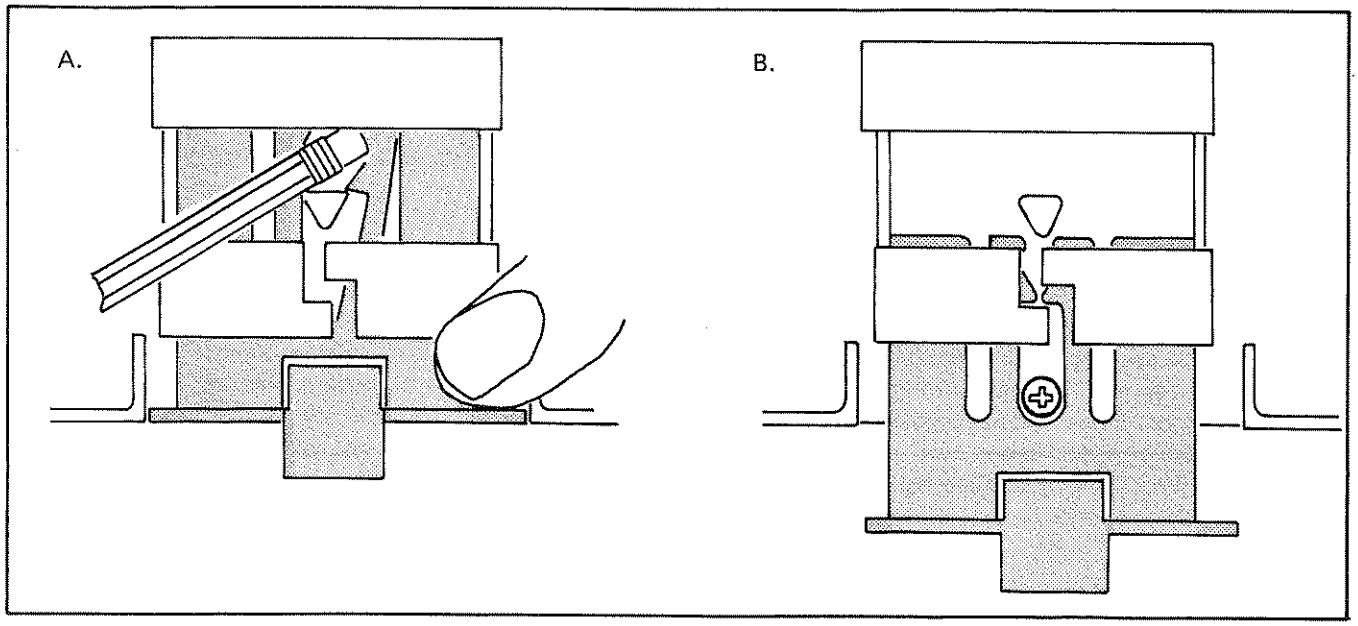


Figure 4-1. Latch Removal

5. Remove the Signal Conditioner Assemblies (A3 and A4) from connectors on the Main PCB and the Front Panel PCB. Pry either assembly gently away from its Front Panel Connector until free. With a gentle rocking motion, now lift the assembly out of its Main PCB connector. Avoid bending individual connector pins on the Signal Conditioners.

NOTE

The Signal Conditioners must not be interchanged. Each assembly is component matched to a hysteresis resistor on the Main PCB.

6. To remove the Front Panel Assembly (A2) from the Main PCB Assembly, first pull off the following switch buttons in the panel's lower left corner:

a. ON- STBY (green).
b. BAT - LINE (white).
c. RESET (blue).

7. Gently pry the Front Panel Assembly away from its 40-pin connector (left) and guide pin (right). Avoid bending individual connector pins on the Main PCB.

8. Refer to Section 6 of this manual when removing any optional assemblies.

4-9. Reassembly

4-10. For reassembly, the disassembly procedures can generally be followed in reverse. Keep the following considerations in mind:

1. When reinstalling the Signal Conditioners or the Front Panel Assembly, care should be taken not to bend the connector pins.

2. When reconnecting the top and bottom case halves, ensure that the Front and Rear Panels fit into their appropriate grooves in the case top half. Slide the top half into place uniformly. Firmly squeeze top and bottom together (at front and rear), and reinstall the six securing screws.

NOTE

Proper RFI shielding depends on top and bottom case halves being securely mated.

4-11. Input Power

4-12. Input line power voltage is selected by positioning the two switches in the right rear corner of the Main PCB. Each switch (S4 and S5) shows a position identifying red or white dot. Line voltage settings identified by dot color are presented in Figure 4-2. Factory line voltage settings are identified on the instruments's rear panel; one of four (4) white dots will be darkened to signify 100, 120, 220 or 240V selection.

4-13. Fuse Replacement

WARNING

DISCONNECT THE INSTRUMENT FROM LINE POWER BEFORE ATTEMPTING FUSE REPLACEMENT.

4-14. The 7250A line power fuse is accessible on the rear panel. Fuse requirements are a 1/4 MDL (slo-blo) for line inputs of 100V or 120V and a 1/8A MDL (slo-blo) for line inputs of 220V or 240V.

4-15. Channel A and Channel B inputs are fuse protected for maximum inputs of 250 mA. Replacement of either of these fuses necessitates removal of the Main PCB Assembly and the Front Panel PCB Assembly; refer to Instrument Disassembly for removal instructions. Each fuse is soldered to the Front Panel PCB Assembly immediately below the respective BNC input connector. Replacement fuses should be ordered from John Fluke Mfg. Co., Inc.

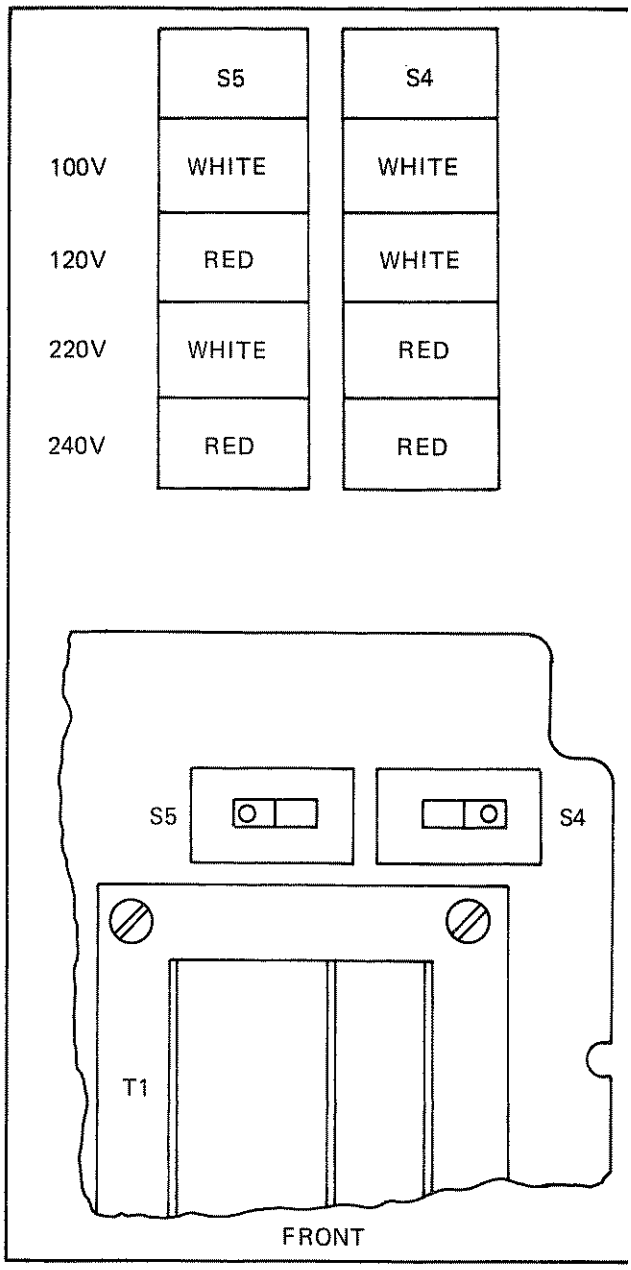


Figure 4-2. Line Voltage Selection

4-16. Cleaning

4-17. Clean the instrument periodically to remove dust grease and other contamination. Use the following procedure:

CAUTION

Do not use aromatic hydrocarbons or chlorinated solvents for cleaning. They will react with plastic materials used in manufacture of the instrument.

1. Clean the front panel and case with soft cloth dampened with a mild solution of detergent and water.

2. Clean the surface of the PCB using clean, dry air at low pressure (≤20 psi). If grease is encountered, spray with Freon T.F. Degreaser or anhydrous alcohol and remove grime with clean, dry air at low pressure.

4-18. PERFORMANCE TEST

4-19. This Performance Test provides a method of verifying overall operation of the 7250A. The test procedures may be used for initial acceptance, for periodic maintenance and evaluation after repair, or as an aid in troubleshooting. If the 7250A should fail any portion of the Performance Test, refer to applicable Calibration procedures and Troubleshooting techniques presented elsewhere in this section. Refer to Table 4-1, List of Recommended Test Equipment, when specific test equipment is called for during the Performance Test.

4-20. Equipment Preparation

4-21. The following checks and set-up procedures should be completed prior to use of the Performance Tests.

1. Ensure that the line cord is connected to the 7250A.

2. Check that the Rear Panel INT/EXT switch is set to INT.

3. Check for the following Front Panel control settings:

BAT/LINE - LINE
STBY/ON - ON
SEP/COM - SEP
FILTER - OUT
ATTENUATION - fully counterclockwise (both channels)
X1 X10 - X1 (both channels)
OFFSET CONTROL - ∿ (both channels)
SLOPE - Negative (pushed in) - both channels

4-22. Time Base Accuracy Test

4-23. The 7250A time base accuracy is a function of the ambient temperature, the line voltage variation, and the time interval since last calibration. Specifications for these factors are presented in Table 1-3 for all available time bases. To check instrument accuracy, use the following procedure:

1. Complete Equipment Preparation and make the following additional control settings:

FUNCTION - FREQ A
RESOLUTION - 1 Hz

2. Connect a 5 MHz 100 mV rms signal from the Low Frequency Synthesizer to Channel A input. The display should read 5000.000 kHz ± 1 count ± time base error.

3. Set the RESOLUTION control to 0.1 Hz. The display should read 000.0000 kHz ± count, ± time base error (OVFL LED on).

4. Compare the display to the maximum allowable deviation in Hz presented in Table 4-2.

5. The allowable deviation in Hz is applicable if calibration has been performed within the preceding month. The deviation can also be compared to the last Time Base Accuracy Test results. In any event, if the new test results are sufficient for the accuracy required by the user, calibration need not be done. If the results are not sufficient, refer to CALIBRATION procedures in this section.

Table 4-2. Maximum Allowable Deviation

TIME BASE TYPE	FREE AIR	TCXO OPTION -112	OVEN OPTION -131	OVEN OPTION -132
Total Time Base Accuracy *	+/–56 X 10^{-7}	+/–23.2 X 10^{-7}	2.2 X 10^{-7}	8.4 X 10^{-8}
Maximum Allowable Deviation ** (with 5 MHz input)	+/–28.0 Hz	+/–11.6 Hz	+/–1.1 Hz	+/–0.5 Hz

* Includes aging rate, temperature effects, line voltage variation.
** Allowable deviation in Hz is found by multiplying the input frequency (5 MHz in this case) by the total accuracy, and adding 1 count error. These figures apply when in 0.1 Hz RESOLUTION.

4-24. Sensitivity Test, Channel A

4-25. This test will verify that Channel A meets sensitivity specifications presented in Table 1-3. Recommended test equipment can be found in Table 4-1. Use the following test procedure:

1. Complete Equipment Preparation and set additional front panel controls as follows:

FUNCTION - FREQ A
RESOLUTION - 0.1 Hz

2. Connect the Low Frequency Synthesizer and the 7250A as illustrated in Figure 4-3 (A).

3. Energize all equipment and allow for appropriate warmup time.

4. Set the Low Frequency Synthesizer to 10 Hz at 100 mV rms; check for a proper display on the 7250A.

5. Reduce the synthesizer output through 10 mV rms; the instrument should maintain a stable display.

6. Repeat steps (4) and (5), this time at a setting of 100 kHz.

7. Set the 7250A RESOLUTION to 1 Hz, and repeat steps (4) and (5) at a frequency of 1 MHz.

8. Disconnect the Low Frequency Synthesizer.

9. Connect the High Frequency Synthesizer, 7250A and RMS Voltmeter with RF Probe and 50Ω Adapter as illustrated in Figure 4-2 (B).

10. Set the synthesizer to 20 MHz at 150 mV rms. Observe a stable display on the 7250A.

11. As the input is reduced through 10 mV rms, the display should remain stable.

12. Repeat steps (10) and (11) at a frequency of 80 MHz. The display should now remain stable through 15 mV rms.

4-26. Sensitivity Test, Channel B

4-27. Test the sensitivity for Channel B with the following procedure:

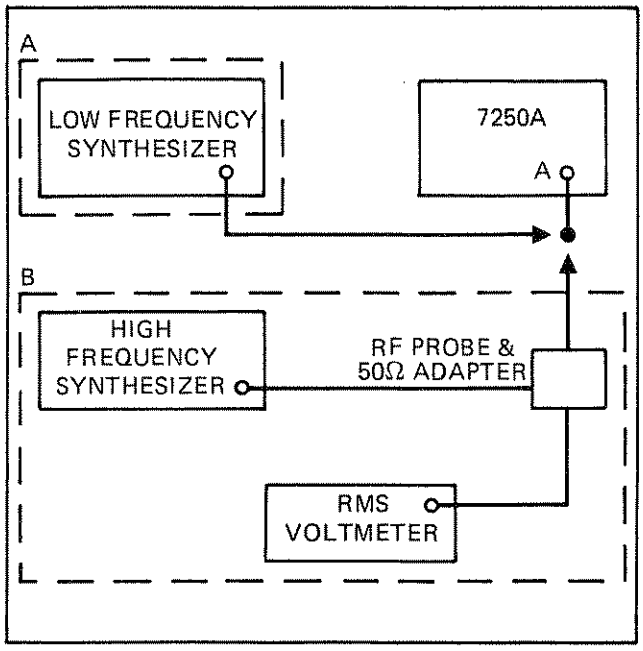


Figure 4-3. Channel A Sensitivity Test Connections

1. Complete Equipment Preparation, and set additional front panel controls as follows:

FUNCTION - RATIO A/B
RESOLUTION - 10^0

2. Connect the High Frequency Synthesizer, 7250A, Low Frequency Synthesizer, and RMS Voltmeter with RF Probe and 50Ω Adapter as illustrated in Figure 4-4.

3. Set the High Frequency Synthesizer (Channel A) to 80 MHz at 100 mV rms.

4. Set the Low Frequency Synthesizer to 10 Hz at 100 mV rms. The 7250A display should read 8000000.

5. Reduce the 10 Hz signal on Channel B until the 7250A stops gating (GATE LED stops flashing). Verify that the level is less than 10 mV. The display will hold the reading made during the last gate.

6. Successively change the Low Frequency Synthesizer settings and the 7250A RESOLUTION settings as defined in Table 4-3. Repeat steps (4) and (5) for each frequency change. Correct display readings should be as presented in Table 4-3.

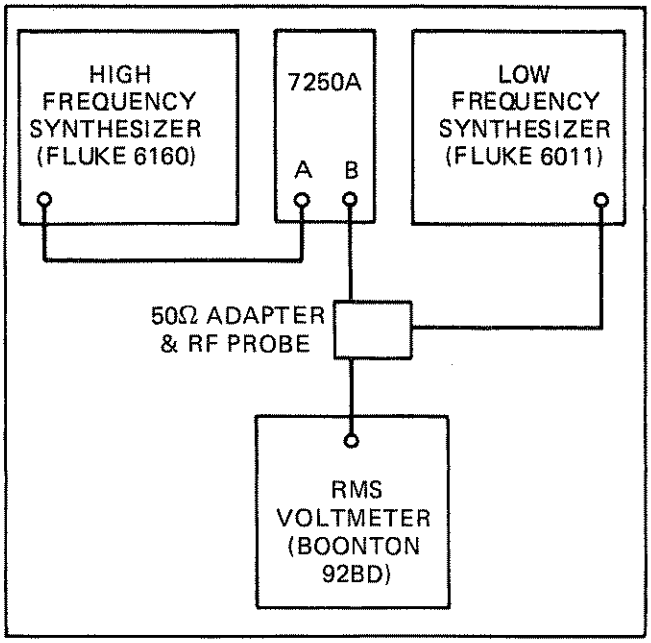


Figure 4-4. Channel B Sensitivity Test Connections

Table 4-3. Channel B Sensitivity Test

LOW FREQUENCY SYNTHESIZER SETTING	7250A RESOLUTION	7250A DISPLAY
10 Hz	10^0	8000000
10 kHz	10^3	8000.000
100 kHz	10^4	800.0000
1 MHz	10^5	80.00000

4-28. Display Test

4-29. The following procedures will verify proper decimal point placement, measurement unit annunciation and scaling factor operation without an input signal. To verify individual display digit operation, perform "Totalize Test".

1. Complete Equipment Preparation.

2. Place the FUNCTION control in FREQ A. Verify that the display digits and measurement unit annunciators appear as defined in Table 4-4 for each RESOLUTION setting.

NOTE

RESET the 7250A after each check in AUTO.

3. Place the FUNCTION control in CPM X100 A. On all RESOLUTION settings, the measurement units annunciators should be blank, and the display should read: 0.

4. Sequence the FUNCTION control through each of the next four positions (RATIO A/B, PER A, PER AVG A, T.I. A-B). Verify correct display digit placement and measurement unit annunciation per Table 4-4.

5. Select TOT A with the FUNCTION control. The measurement unit should now be blank and the display should read: 0 (all RESOLUTION settings).

6. Set the FUNCTION control to CHK: verify that display indications match those of Table 4-4. Also check that the display reads "8888888" when the RESET switch is held depressed (all RESOLUTION settings).

4-30. Frequency A Test

4-31. This test will verify operation of the 7250A's digital circuitry, CHANNEL A Signal Conditioner and display digits. Use the following procedure to test the frequency function.

1. Complete Equipment Preparation.

2. Set other controls to:

   FUNCTION - FREQ A
   RESOLUTION - 100 Hz
   ATTENUATION - fully ccw

3. Apply an 8 0 MHz signal to CHANNEL A input from the High Frequency Synthesizer. Monitor the Signal level with an RF Voltmeter and 50Ω Adapter.

4. Vary the input level between 10 mV rms and 1V rms; check for a proper display at all levels.

5. Push the ATTENUATION control in for negative slope; repeat step 4.

6. Make the following control settings:

   ATTENUATION - X10
   SLOPE - + (out)

7. While maintaining a 10 mV rms input, check for a display of 0.

8. Set the input level to 100 mV rms; verify a stable and correct readout.

Table 4-4. Display Test

FUNCTION		DISPLAY FOR AVAILABLE RESOLUTION SETTINGS						
		1	2	3	4	5	6	
FREQ A	RESOLUTION	10 kHz	1 kHz	100 Hz	10 Hz	1 Hz	0.1 Hz	AUTO
	READOUT	0.00	0.000	0.0000	0.00	0.000	0.0000	0.000
	ANNUNCIATOR	MHz	MHz	MHz	kHz	kHz	kHz	kHz
RATIO A/B	RESOULTION	10^0	10^1	10^2	10^3	10^4	10^5	AUTO
	READOUT	0	.0	.00	.000	.0000	.00000	0
	ANNUNCIATOR	(none)	(none)	(none)	(none)	(none)	(none)	(none)
PER A	RESOLUTION	100 ns	1 μs	10 μs	100 μs	1 ms	10 ms	AUTO
	READOUT	0.0000	0.000	0.00	0.0000	0.000	0.00	0.00
	ANNUNCIATOR	ms	ms	ms	s	s	s	ms
PERIOD AVERAGE (PER AVG A)	RESOLUTION	10^0	10^1	10^2	10^3	10^4	10^5	AUTO
	READOUT	0.0000	0.00000	0.000	0.0000	0.00000	0.000000	0.0000
	ANNUNCIATOR	ms	ms	μs	μs	μs	μs	ms
TI A-B	RESOLUTION	100 ns	1 μs	10 μs	100 μs	1 ms	10 ms	AUTO
	READOUT	0.0000	0.000	0.00	0.0000	0.000	0.00	0.00
	ANNUNCIATOR	ms	ms	ms	s	s	s	ms
SELF CHECK	RESOLUTION	10 kHz	1 kHz	100 Hz	10 Hz	1 Hz*	0.1 Hz*	AUTO
	READOUT	10.00	10.000	10.0000	10000.00	0000.000	000.0000	10000.00
	ANNUNCIATOR	MHz	MHz	MHz	kHz	kHz	kHz	kHz

* OVFL Annunciator ON.

9. Set CHANNEL A ATTENUATION to X1.

10. While maintaining a 10 mV rms input from the High Frequency Synthesizer, verify stable and correct readings at frequencies of 1, 5 and 20 MHz. Set the synthesizer to 15 mV rms, and check for stable readings at 50 and 80 MHz.

11. Connect the Low Frequency Synthesizer to CHANNEL A input.

12. Set the 7250A RESOLUTION control to 1 Hz.

13. While maintaining a constant input level of 10 mV rms, verify stable and correct readings at frequencies of 10, 100, 1000 Hz.

14. Set the RESOLUTION control to 10 Hz.

15. While maintaining an input level of 10 mV rms, verify stable and correct readings at frequencies of 10, 50 and 500 kHz.

4-32. Counts Per Minute Test

4-33. Use the following procedure to verify 7250A operation in the CPM X100A function:

1. Complete Equipment Preparation.

2. Set additional controls as follows:

   FUNCTION - CPM X100A
   RESOLUTION - 0.1 Hz
   FILTER - IN

3. Apply a 5 kHz, 10 mV rms signal to CHANNEL A input from the Low Frequency Synthesizer.

4. The display should read 3000, with no decimal point or measurement unit.

5. Shift the RESOLUTION control through all remaining settings. The display should remain unchanged.

4-34. Ratio Test

4-35. Use the following procedure to verify operation in the RATIO A/B function:

1. Complete Equipment Preparation.

2. Set other controls as follows:

   FUNCTION - RATIO A/B
   RESOLUTION - 10 kHz
   SEP/COM - COM

3. Apply a 1 kHz, 1V rms signal from the Low Frequency Synthesizer to CHANNEL A input; verify a reading of 1.

4. Change the input signal to 1 MHz at 1V rms; verify a reading of 1.

5. Change the RESOLUTION setting to 0.1 Hz and verify a reading of 1.00000.

4-36. Period Test

4-37. Use the following procedure to check 7250A operation in the PER A function:

1. Complete Equipment Preparation.

2. Set additional controls as follows:

   FUNCTION - PER A
   RESOLUTION - 10 kHz

3. Apply a 1 kHz, 1V rms signal from the Low Frequency Synthesizer to CHANNEL A input. Check for a stable 7250A display of 1.0000 ms (± signal generator instability).

4. Apply a 2 MHz signal at 1V rms to CHANNEL A input; check for a stable display of 0.0005 ms (± 1 count).

4-38. Period Average Test

4-39. Use the following procedure to verify operation in the PER AVG A function.

1. Complete Equipment Preparation.

2. Set additional controls as follows:

   FUNCTION - PER AVG A
   RESOLUTION - 10 kHz

3. Apply a 10 kHz, 1V rms signal from the Low Frequency Synthesizer to CHANNEL A input. The display should read 0.1000 ms.

4. Set the RESOLUTION control to 0.1 Hz.

5. Apply a 1.5 MHz, 1V rms signal to CHANNEL A input. Check for a stable display of 0.666666 μs (± time base error).

4-40. Time Interval Test

4-41. Use the following procedure to check for correct operation of the T.I. A-B function:

1. Complete Equipment Preparation.

2. Set additional controls as follows:

   FUNCTION - T.I. A-B
   RESOLUTION - 1 kHz
   SEP/COM - COM

3. Set the Low Frequency Synthesizer to 1 kHz.

4. Connect TTL OUT (on the Synthesizer) to CHANNEL A input on the 7250A.

5. Set CHANNEL A and B slope switches to "+" and check for a display of "1.000 ms".

4-42. Totalize Test

4-43. Use the following procedure to verify 7250A operation in the TOT A function:

1. Complete Equipment Preparation.

2. Set additional controls as follows:

   FUNCTION - TOT A

3. Remove any inputs from CHANNEL A. The GATE LED should be on.

4. Depress the RESET switch; the display should reset to 0.

5. Apply a 10 Hz signal (at 1V rms) to CHANNEL A input. Observe a proper count sequence and digit segment illumination for digits one and two.

6. Check digits 3 through 7 in a similar manner, increasing the frequency by 10 for each successive digit.

7. Check that the OVFL LED illuminates when digit 7 changes from 9 to 0.

4-44. Self Check Test

4-45. Use the following procedure to verify proper operation of 7250A when in the CHK function:

1. Complete Equipment Preparation.

2. Make the following additional control settings:

   FUNCTION - CHK
   RESOLUTION - 10 Hz

3. Check for a display of 10000.00 kHz (±1 count). Verify that the GATE LED flashes approximately 5 times per second.

4. Hold the RESET switch depressed. The display should read 88888.88 kHz and the GATE LED should stop flashing while RESET is held depressed.

4-46. CALIBRATION

4-47. Calibration for the 7250A consists of Time Base and trigger level adjustments. These adjustments should be made after repairs are completed or whenever the instrument fails to meet PERFORMANCE TEST requirements.

4-48. Time Base Calibration

4-49. Calibration should be made whenever the time base is repaired or replaced, or when it is determined that instrument accuracy is not within the accuracy desired. The Time Base Accuracy Test can be used as an initial accuracy determination. Perform the Time Base adjustment in an environment having an ambient temperature between 20° C and 30° C (68° F to 86° F). Use the following procedure when calibrating the time base:

1. The 7250A must be operating for 5 minutes with top and bottom covers installed prior to calibration.

2. Set front panel controls on the 7250A as follows:

   FUNCTION - FREQ A
   RESOLUTION - 1 Hz
   SEP/COM - SEP
   FILTER - OUT
   ATTENUATION - X1, fully ccw

3. Connect a 5 MHz, 100 mV rms signal from the Low Frequency Synthesizer to Channel A input.

4. If necessary, adjust the time base for a displayed reading of 50000.000 kHz (± 1 count). This adjustment is accessed through a hole in the left rear of the bottom case half (see Figure 4-5). Use JFD 5284 (or equivalent) non-ferrous adjustment tool. If installed at the rear of the bottom case half, the bail will have to be removed to allow access.

5. Once optimum adjustment has been attained in Step (4), the RESOLUTION control can be placed to 0.1 Hz; adjustment can now be made toward a displayed reading of 000.0000 kHz. The OVFL LED will be on during this procedure. Since the gate time in this setting is 10s, the effect of each fine adjustment will not be immediately noticed.

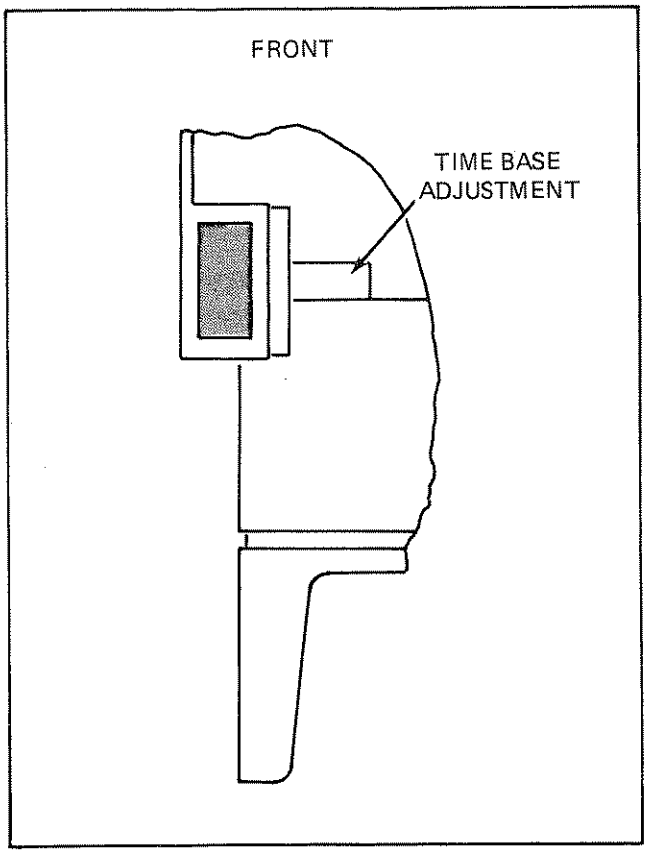


Figure 4-5. Time Base Adjustment

4-50. Coarse Time Base Adjustment

4-51. Some versions of the Free Air Time Base will have an additional coarse adjustment control. This control is located on top of the time base and is accessible only with the 7250A's top case half removed.

NOTE

Do not perform coarse adjustment unless Time Base Calibration steps 1 - 5 fail to bring the instrument within specifications.

If coarse adjustment is determined necessary, use the following procedure:

1. Set the fine adjustment, accessed through the bottom case half, to mid range.

2. Remove the instrument's top cover (see Disassembly).

3. Perform steps (2) and (3) of Time Base Calibration.

4. Use a non-ferrous alignment tool to adjust the coarse control for a display as close as possible to 5000.000 kHz.

5. Replace the top case half (see Reassembly) and perform Time Base Calibration.

4-52. Channel A Trigger Level Adjustment

4-53. Use the following procedure when adjusting the Channel A trigger level:

1. Complete Equipment Preparation and set additional front panel controls as follows:

   FUNCTION - FREQ A
   RESOLUTION - 100 Hz
   SLOPE ± (CHANNEL A)

2. Connect a 10 MHz, 10 mV rms signal from the Low Frequency Synthesizer to Channel A input.

3. Connect an oscilloscope to U8-4, and look for a TTL waveform representative of the input frequency.

4. If necessary, adjust R34 to obtain a 50% duty cycle.

5. Disconnect the oscilloscope and the Low Frequency Synthesizer.

6. Connect an 80 MHz, 15 mV rms signal from the High Frequency Synthesizer to Channel A input. Monitor the signal level with an RF Voltmeter and 50Ω Adapter.

7. Look for a stable display of 80.0000 MHz. If neccessary, adjust R34 slightly to obtain a stable reading.

4-54. Channel B Trigger Level Adjustment

4-55. Use the following procedure when adjusting the Channel B trigger level:

1. Complete Equipment Preparation and set additional front panel controls as follows:

   FUNCTION - RATIO A/B
   RESOLUTION - 0.1 Hz

2. Connect a 1 MHz, 100 mV rms signal from the Low Frequency Synthesizer to Channel B input.

3. Connect an oscilloscope to U8-6 and look for a TTL wave form representative of the input frequency.

4. If necessary, adjust R26 to obtain a 50% duty cycle.

5. Connect an 80 MHz, 15 mV rms signal from the High Frequency Synthesizer to Channel A input. Change RESOLUTION to 10 Hz. Monitor Channel A input levels with an RF Voltmeter and 50Ω Adapter.

6. Disconnect the oscilloscope and look for a stable display of 80.000, if necessary, adjust R26 slightly to obtain a flashing GATE LED and a stable display (± time base error).

4-56. SELECTED COMPONENT REPLACEMENT

4-57. Each Signal Conditioner Assembly is matched with a selected hysteresis resistor. This resistor, mounted on the Main PCB, is designated R32 for Channel A and R35 for Channel B. If a replacement Signal Conditioner is accompanied with a resistor differing in value from the original, the new resistor must be installed.

4-58. TROUBLESHOOTING

4-59. The information given in the following paragraphs is provided to assist in isolating malfunctions in the 7250A. Before troubleshooting the instrument, however, it should be verified that the cause for the malfunction is actually in the instrument and not caused by faulty external equipment or improper control settings. For this reason, the PERFORMANCE TEST is suggested as the first step in troubleshooting. The performance test may also help to localize the trouble to a particular section of the instrument.

4-60. The following reminders of basic fault isolation will help determine if the cause is the result of an internal malfunction or faulty external connections.

1. Carefully check the 7250A control settings: some false indications may be caused by an incorrect or overlooked control setting.

2. Check associated equipment: insure that equipment controls and connections are correct.

3. Carefully inspect the interior of the instrument: check for physically damaged parts, loose or broken wires and improperly seated plug-in assemblies.

4-61. Several factors should be kept in mind during troubleshooting.

1. A working knowledge of the instrument's operation will be valuable whether or not the tabular flow chart is used. It is recommended that Section 3 of this manual (Theory of Operation) be read before any troubleshooting is done.

2. Different circuit logic levels will be encountered. Circuits handling higher frequencies, such as the Signal Conditioners and the Main PCB channel inputs, employ emitter coupled logic (ECL) and are designated with a "', e.g. dp'. Some Control Logic (U13) lines will be at CMOS levels. Transistor-transistor logic (TTL) comprises most circuitry. Typical logic levels for all three logic types are presented in Table 4-5.

3. Care should be exercised when soldering on printed circuit boards. Excessive heat (soldering tip temperatures above 700°F) can cause unseen damage to the board. Whenever possible, alternate soldering tool usage between divergent areas on the board. Concentration of heat in any one area will thereby be minimized.

4. Observe Static Discharge Precautions whenever working with or around MOS-type integrated circuits. Table 4-6 lists such components by location and type.

5. Incorrect output voltages from any of the power supplies may cause the instrument to exhibit various improper indications. The power supply voltages should be checked in the event of any instrument malfunction.

4-62. There are several recommended methods for troubleshooting circuit loading of a power supply voltage. Checking resistance while removing pcb assemblies and socket-mounted integrated circuits may isolate the loading problem to a particular easily removed unit. Further troubleshooting within these units or on the Main PCB may be accomplished using the following techniques:

Table 4-5. Typical Logic Levels

	LOGIC 1	LOGIC 0
TTL	>2.5V	<0.6V
ECL*	4.1V	3.2V
CMOS	>3.5V (>70% of supply)	<1.5V (<30% of supply)

* All ECL circuits in the 7250A are supplied by +5V.

Table 4-6. MOS Type Integrated CKTS

ASSEMBLY NAME	REF DES	TYPE
Main PCB	U13	Custom
Main PCB	U15	LS7031
Main PCB	U22	4511BE
Signal Conditioner A	A3	
Signal Conditioner B	A4	

1. Resistance: check between supply voltage and ground at the appropriate pins for each integrated circuit. Use precision four-wire resistance measurement techniques and a digital multimeter.

2. Current: use a current probe to detect high current drain at the relevant power supply input pin to each integrated circuit.

3. Temperature: use a temperature probe (such as the Fluke 80T-150) and a digital multimeter to sense over-temperature integrated circuits. Alternately, monitor the supply voltage while successively spraying each integrated circuit with a circuit coolant.

4-63. Static Discharge Precautions

4-64. Static discharge can damage MOS-type integrated circuits found in the 7250A. The following precautions should be observed when conducting adjustments or repairs with the instrument's top cover removed.

1. Never conduct repairs without first pressing power to STBY and disconnecting the line cord.

2. Perform all repairs at a static-free work station.

3. Minimize handling of IC's and the pcb; in no case handle them by their connectors.

4. Keep repair parts in their original containers until ready for use.

5. Use static ground straps to discharge repair personnel.

6. Use conductive foam or anti-static containers to store replacement or removed IC's.

7. Remove all plastic, vinyl and styrofoam products from the work area.

8. Do not slide static sensitive devices over any surface.

9. Use only anti-static type solder removal tools.

10. Use grounded tip soldering irons.

4-61. When it is determined that the malfunction is within the 7250A, the simplified troubleshooting procedures presented in Table 4-7 can be used to isolate the problem area. These procedures are presented as a tabular flow chart. When a step on this chart is completed, check for a decision transfer. If no decision is required, perform the next step in sequence. Refer to Figure 4-6 for test point location and identification. Table 4-1 recommends test equipment to be used when troubleshooting.

Table 4-7. Troubleshooting

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
	Before using the following troubleshooting procedure, check for incorrect or overlooked control settings and instrument connections. *NOTE* *The PERFORMANCE TESTS described in this section may also be used as an aid in troubleshooting the 7250A.*		
1	Perform Equipment Preparation, described under PERFORMANCE TEST in this section.		
2	Does the 7250A's front panel present any visual indication when power is applied?	3	5
3	Is the Gate LED illuminated?	4	26
4	Is there a display? Is the displayed frequency correct?		46 58
5	Verify that power is available at the ac receptacle in use.	6	
6	Check that the power cord is properly attached.	7	
7	Verify that a line fuse appropriate for the supply voltage is installed (the line cord should be disconnected when checking the line fuse).	8	
8	Referring to Instrument Disassembly, remove the 7250A's top cover.		
9	Visually inspect the pcb assemblies for signs of component damage, shorted land patterns or foreign matter.		
10	With the line cord disconnected, connect an ohmmeter between TP3 and ground. Figure 4-6 illustrates test point location. Check for a reading of 400 ohms (+/−100 ohms) in either direction.	15	11
11	With the ohmmeter still connected, remove each Signal Conditioner PCB Assembly. Does the ohmmeter read 650 ohms (+/−100 ohms)?	12	13
	NOTE *Do not bend or touch Signal Conditioner connector pins. Observe static sensitive precautions.*		
12	Replace the Signal Conditioner PCB Assembly removed prior to obtaining the correct ohmmeter reading.		
13	Remove the Front Panel PCB Assembly, and check for the correct ohmmeter reading.	14	15
14	Repair the Front Panel PCB Assembly.		
15	Disconnect the ohmmeter.		

Table 4-7. Troubleshooting (cont)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
16	Connect a voltmeter to U24-2 (HI) and ground (LO). Connect the line cord to the instrument, but leave the power switch in STBY.		
17	Check for +5V at S3-2.	19	18
18	Check U24 and C4.		
19	Place the power switch to ON, and check for +5V.		20
20	Place power to STBY, and remove U13. Place power to ON and check for +5V.	22	21
21	Using the same procedure, remove U15 and check for +5V.	23	24
22	Install a new U13 (Power in STBY).		
23	Install a new U15 (Power in STBY).		
24	Reinstall U13 and U15 (originals) (Power in STBY).		
25	Check for +5V circuit loading at appropriate pins for all other integrated circuits on the Main PCB Assembly. (The following steps should be followed if there is no GATE light.)		
26	Verify that the INT EXT REF switch on the rear panel is set to INT.		
27	Using an oscilloscope, check for the 10 MHz reference frequency signal at U19-2. TTL levels should be present.	38	28
28	Check Q8. Is it good?		29
29	Replace Q8.		
30	If the 7250A is equipped with one of the oven time bases (Options -131 or -132), either the time base or the +5V is defective.		
31	Connect a voltmeter to U24-2 (HI) and ground (LO). Check for +5V.	32	10
32	Replace the oven time base.		
33	If the instrument is equipped with the Free Air Time Base or with the TCXO (Option -112), press the power switch to STBY and disconnect the line cord. Connect an ohmmeter to TP1 and ground, and check for a reading of 1000 +/—100 ohms.		
34	Connect a voltmter to U27-2 (HI) and ground (LO). With the power switch in STBY, connect the line cord.		

Table 4-7. Troubleshooting (cont)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
35	Check for a reading of +12V.	37	36
36	Disconnect the line cord. Check U27 and C1.		
37	Replace the Free Air Time Base (or TCXO, if installed).		
38	Check for 1 MHz at U13-12.	39	
39	Connect a voltmeter to TP2 (HI) and ground (LO). Check for a reading of −12V.		40
40	Replace U13, and again check for −12V at TP2.		
41	Set the front panel RESOLUTION to "100 ns". Check at U5-4 and U5-15 for a high when the front panel RESET switch is momentarily depressed.	43	42
42	Replace U14.		
43	Check for a high (dependent on gate time) at U5-5.	45	44
44	Replace Main Gate Flip-Flop U5.		
45	Check circuitry between U5-5 and U5-11.		
	(The following steps should be followed if there is a gate light, but no display.)		
46	Select the CHK function and look for a 10 MHz signal at U5-13.	49	47
47	Check for a 10 MHz signal at U10-6, U10-3 and U10-11.		48
48	Replace U10.		
49	Set the front panel RESOLUTION control to "0.1 Hz". Check for 5 MHz at U5-9.	51	50
50	Replace U5.		
51	Check for ÷5 BCD output from U4.	53	52
52	Replace U4.		
53	Check for ÷10 BCD output from U9.	55	54
54	Replace U9.		
55	Check at U15-9 for the strobe output (approximately 500 Hz with a 10% duty cycle).	57	56
56	Replace U15.		

Table 4-7. Troubleshooting (cont)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
57	Check display driver and decoder circuits U16, U17 and U22. (The following steps should be used if the instrument improperly displays the input frequency.)		
58	Set the 7250A FUNCTION control to FREQ A. Connect a 1 MHz, 1V p-p signal to CHANNEL A input. Is the frequency displayed?		59
59	Disconnect the power cord, and remove the 7250A's top cover. Connect a voltmeter to TP4 (HI) and ground (LO). Connect the power cord, press the power switch to ON, and check for −5V.	60	
60	Press the power switch to STBY, and check for −5V at S3, pin 5.		61
61	Check C3.		
62	Disconnect the line cord, Remove the Channel A Signal Conditioner (avoid bending connector pins).		
63	Energize the 7250A and check for approximately −13V.	64	
64	Replace the Channel A Signal Conditioner.		
65	Repeat steps 59, 60 and 61 for the Channel B Signal Conditioner.		
66	Set the CHANNEL A ATTENUATION controls to minimum (X1, fully ccw).		
67	Apply a 1 MHz, 1V p-p signal to the CHANNEL A input.		
68	Monitor the input signal at pin 8 of the Channel A Signal Conditioner.	70	69
69	Check the Channel A input fuse, input capacitor and input switch.	70	
70	Check at the base of Q1 for the 1 MHz signal.		71
71	Replace the Channel A Signal Conditioner. (Use the following steps if the 7250A does not count high frequencies properly.)		
72	Ensure that the following control settings are made: Filter OUT Sep-Com to SEP		
73	Perform the Trigger Level Adjust described in CALIBRATION. Does the 7250A measure 80 MHz properly?		74
74	Check outputs from U4, U9 and U15 for proper counter action.		

Table 4-7. Troubleshooting (cont)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
	(Use the following steps if the 7250A does not operate properly in CPM mode.)		
75	Check for 1/6 MHz at U13-12.	76	77
76	Check for proper decoding of CPM commands at U14-11.		
77	Check for 1/6 MHz at U6-6 and U6-4.		78
78	Replace U6.		
	(Use the following steps if RATIO A/B mode does not operate.)		
79	Apply a 1 MHz, 1V p-p signal to CHANNEL B input.		
80	Monitor the input signal at pin 8 of the Channel B Signal Conditioner.	82	81
81	Check the Channel B input fuse, input capacitor and input switch.		
82	Check for the 1 MHz signal at the collector of Q9.		83
83	Replace the Channel B Signal Conditioner.		

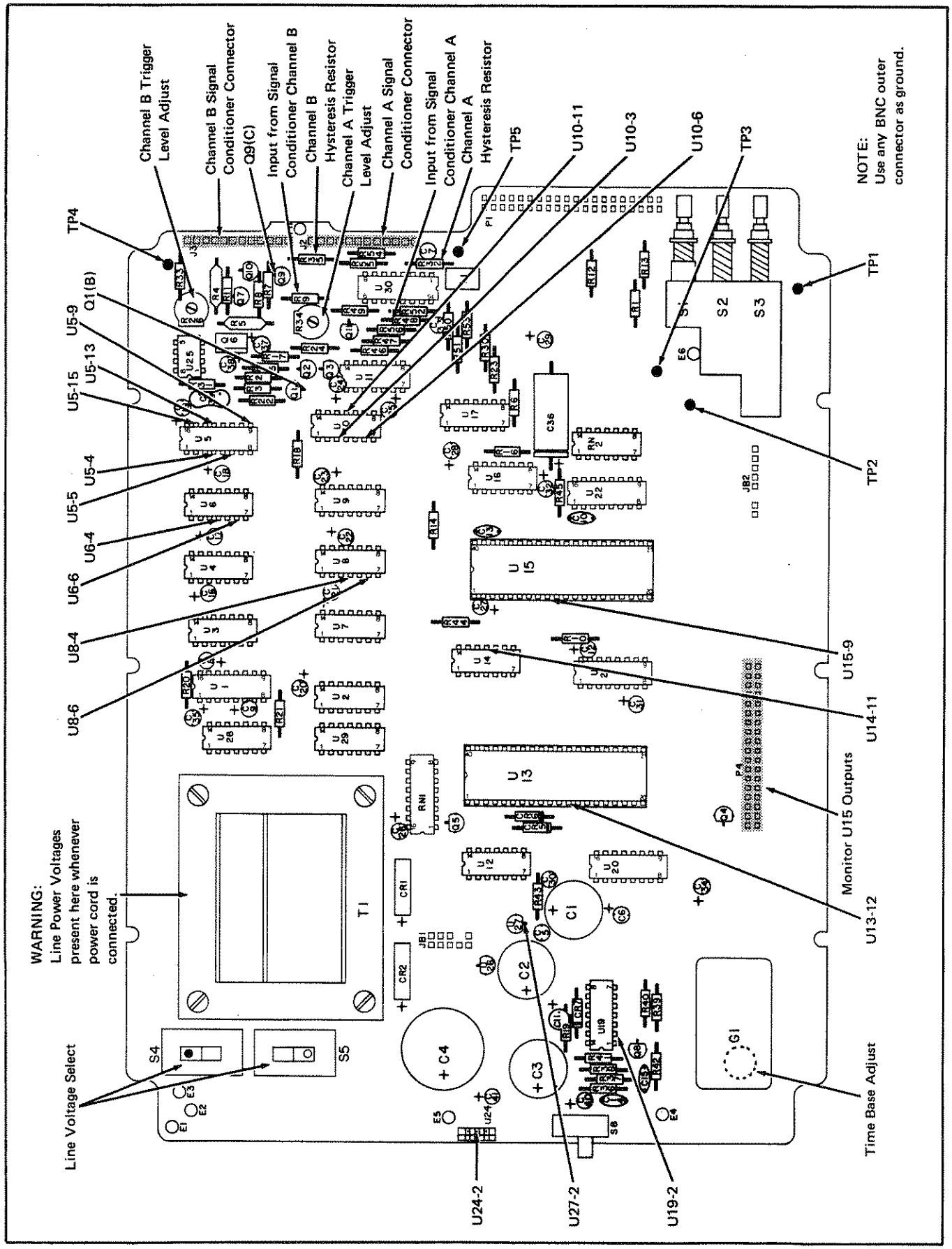


Figure 4-6. Maintenance Locator

Section 5
List of Replaceable Parts

TABLE OF CONTENTS

1 A3/A4 Assemblies; See Final Assembly Parts List

5-1. INTRODUCTION

5-2. This section contains an illustrated parts breakdown of the instrument. A similar parts listing for each of the Options will be found in Section 6. Components are listed alphanumerically by assembly. Both electrical and mechanical components are listed first by reference designation and second by item number. Each listed part is shown in an accompanying illustration.

5-3. Parts lists include the following information:

1. Reference Designation or Item Number.

2. Description of each part.

3. FLUKE Stock Number.

4. Federal Supply Code for Manufacturers. (See Section 7 for Code-to-Name list.)

5. Manufacturer's Part Number or Type.

6. Total Quantity per assembly or component.

7. Recommended Quantity: This entry indicates the recommended number of spare parts necessary to support one to five instruments for a period of two years. This list presumes an availability of common electronic parts at the maintenance site. For maintenance for one year or more at an isolated site, it is recommended that at least one of each assembly in the instrument be stocked. In the case of optional subassemblies, plug-ins, etc., that are not always part of the instrument, or are deviations from the basic instrument model, the REC QTY column lists the recommended quantity of the item in that particular assembly.

5-4. HOW TO OBTAIN PARTS

5-5. Components may be ordered directly from the manufacturer by using the manufacturer's part number, or from the John Fluke Mfg. Co., Inc. factory or authorized representative by using the FLUKE STOCK NUMBER. In the event the part you order has been replaced by a new or improved part, the replacement will be accompanied by an explanatory note and installation instructions if necessary.

5-6. To ensure prompt and efficient handling of your order, include the following information.

1. Quantity.

2. FLUKE Stock Number.

3. Description.

4. Reference Designation or Item Number.

5. Printed Circuit Board Part Number.

6. Instrument Model and Serial Number.

CAUTION

Indicated devices are subject to damage by static discharge.

Table 5-1. Final Assembly 7250A

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	⊘ FINAL ASSEMBLY, 7250A FIGURE 5-1 (7250A-5001)						
A1	⊘ MAIN PCB ASSY	476689	89536	476689	1		
A2	FRONT PANEL PCB ASSEMBLY				1		
A3	⊘ SIGNAL CONDITIONER	479964	89536	479964	2		
A4	⊘ SIGNAL CONDITIONER [1]	479964	89536	479964	REF		
A5	TIMEBASE PCB ASSEMBLY	406918	89536	406918	1		
F1	FUSE, MDL, 1/4A, SLO-BLO, (100V)	166306	71400	MDL1-4	1		5
	FUSE, MDL, 1/8A, SLO-BLO, (220V)	166488	71400	MDL1-4			
H1	GROMMET	104273	72653	7582	1		
H2	NUT, 4-40	110635	73734	8003N	1		
H3	NUT, SELF-LOCK, 6-32	152819	78189	511-310110-60	4		
H4	SCREW, PHP/SS, 4-40 X 1/4	185918	89536	185918	2		
H5	SCREW, PHP 4-40 X 5/16	114876	89536	114876	6		
H6	SCREW, THD FRM, 6-20 X 3/8	288266	89536	288266	1		
H7	SCREW, FHP, 6-35 X 5/8	114876	89536	114876	6		
H8	WASHER, SPLIT, #4	110395	89536	110395	1		
H9	WASHER	175943	89536	175943	1		
MP1	CONNECTOR, BNC	152033	02660	UG1094A/U	1		
MP2	COVER, CONNECTOR	488395	89536	488395	1		
MP3	ASSY, BOTTOM COVER	489302	89536	489302	1		
MP4	COVER, TOP	489310	89536	489310	1		
MP5	DECAL, SPECIAL	483065	89536	483065	1		
MP6	LATCH	467548	89536	467548	1		
MP7	NAMEPLATE, SERIAL (NOT SHOWN)	472795	89536	472795	1		
MP8	PANEL, REAR	476713	89536	476713	1		
MP9	PUSHBUTTON, BLUE	486472	89536	486472	1		
MP10	PUSHBUTTON, LITE GREY	486480	89536	486480	1		
MP11	PUSHBUTTON, GREEN	486498	89536	486498	1		
MP12	BUTTRESS, SUPPORT	481796	89536	481796	1		
MP13	LABEL, WARNING	386250	89536	386250	1		
T1	TRANSFORMER	486514	89536	486514	1		
W1	LINE CORD (NOT SHOWN)	343723	70903	PH290B	1		
W2	CABLE ASSEMBLY	475228	89536	475228	1		
XF1	FUSEHOLDER, NUT	460329	89536	460329	1		
	FUSEHOLDER CAP (W/XF1)	460238	89536	460238	1		
	INSTRUCTION MANUAL (NOT SHOWN)	487496	89536	487496			

[1] A3/A4 must be ordered at pcb level only. A3 is matched to R32, A4 is matched to R35 on A1 Main PCB Assemlby. No parts breakdown will be listed. For placement see Final Assembly, Figure 5-1.

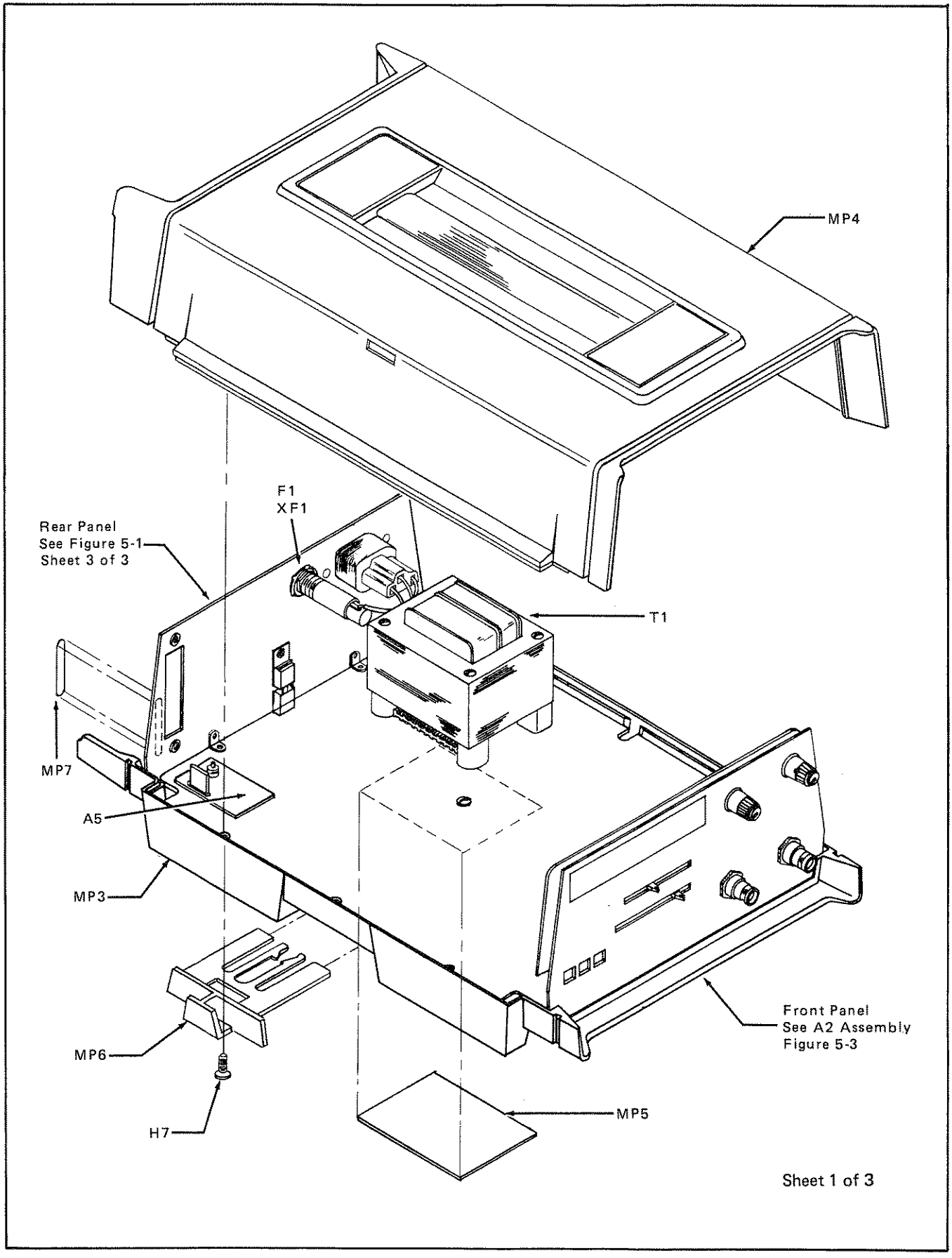


Table 5-1. Final Assembly

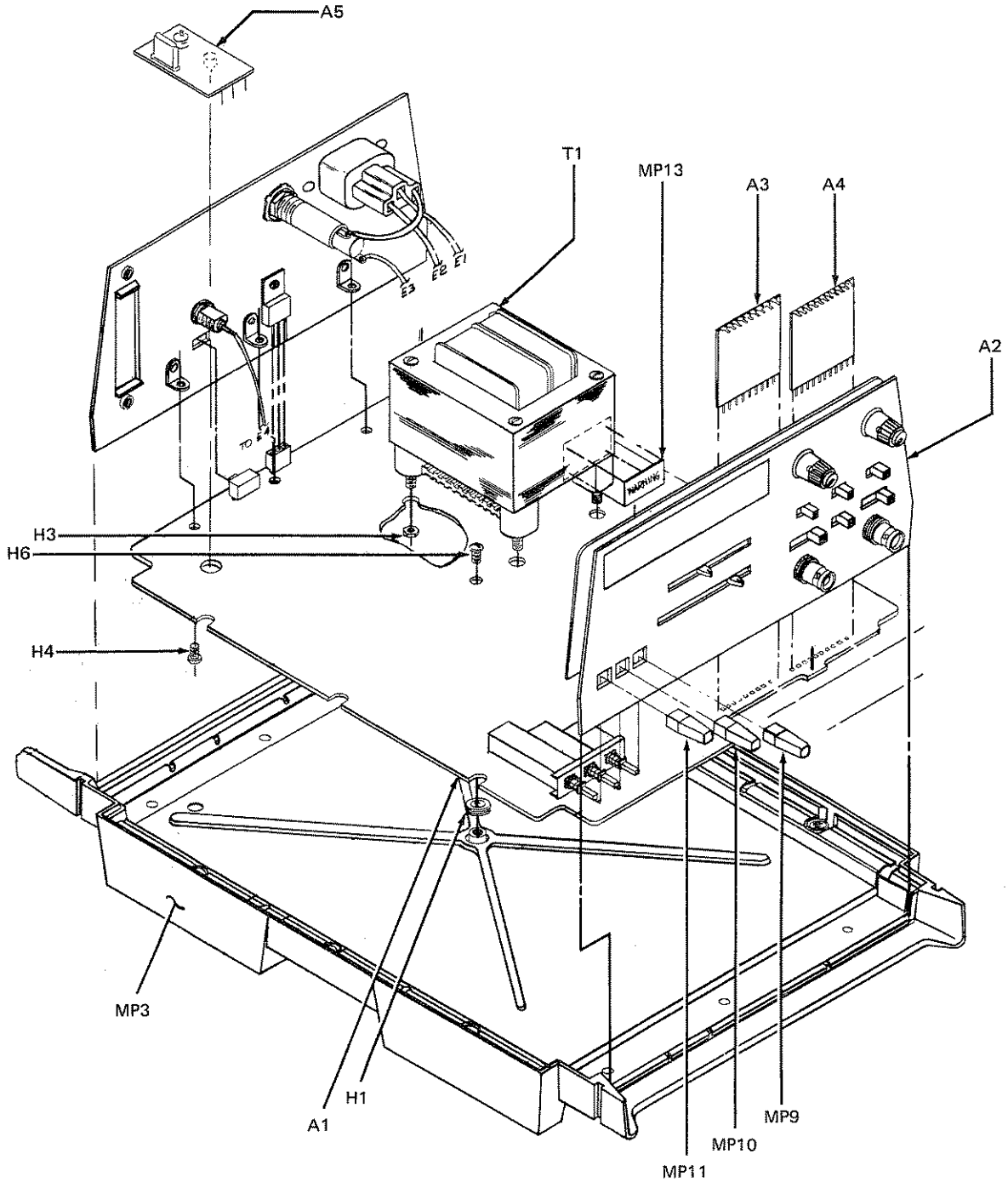


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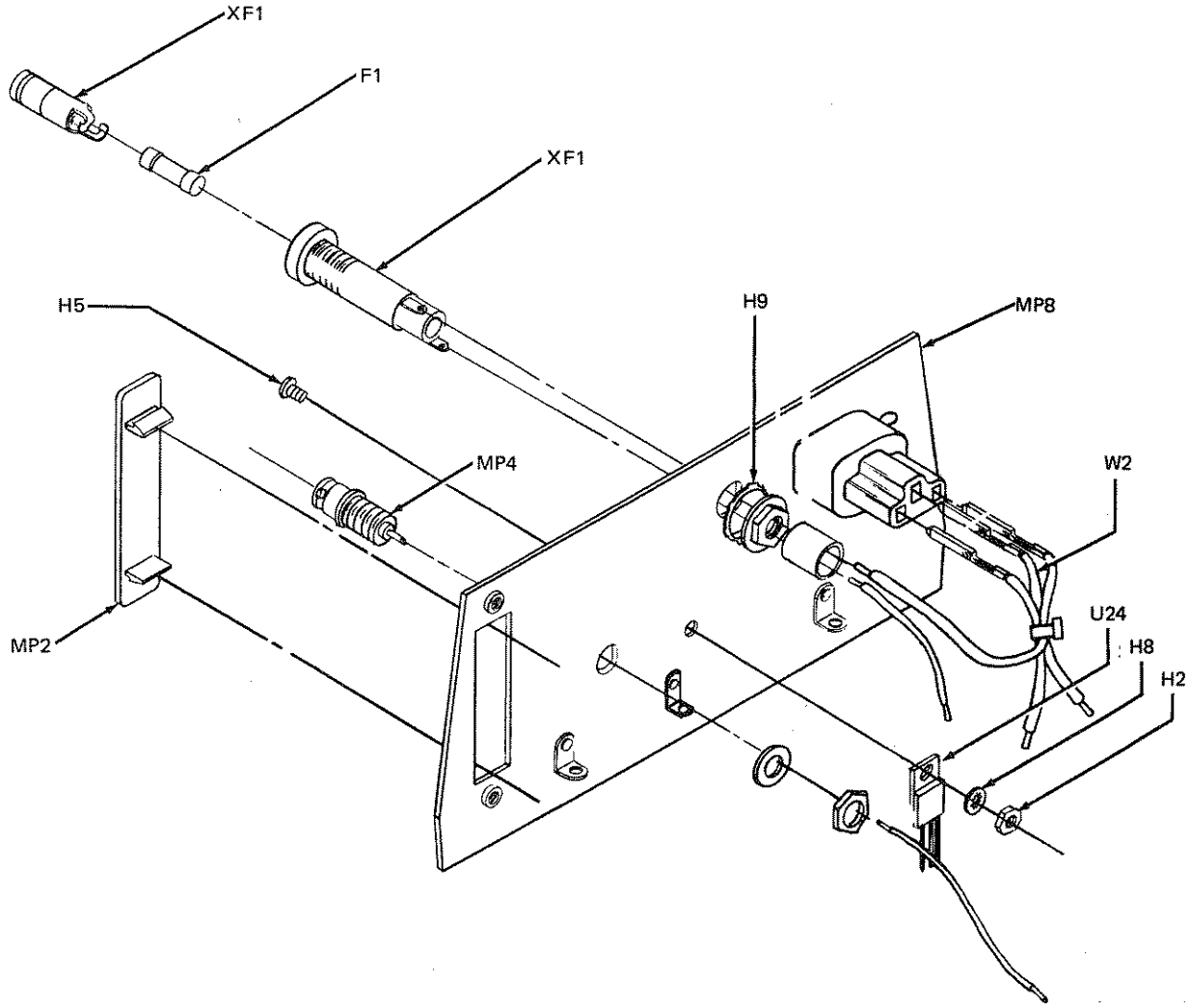
Figure 5-1. Final Assembly (cont)



REAR PANEL SECTION

Sheet 3 of 3

Figure 5-1. Final Assembly (cont)

Table 5-2. A1 Main PCB Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
A1	Ⓐ MAIN PCB ASSEMBLY FIGURE 5-2 (7250A-4001T)	476689	89536	476689	REF		
C1	CAP, ELECT, 470 UF -10/+75%, 35V	478792	89536	478792	2		
C2	CAP, ELECT, 470 UF -10/+75%, 35V	478792	89536	478792	REF		
C3	CAP, ELECT, 1000 UF -10/+75%, 25V	478826	89536	478826	1		
C4	CAP, ELECT, 4700 UF -10/+75%, 15V	460261	80031	3143TS502V015	1		
C5	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	7		
C6	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C7	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C8	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	22		
C9	CAP, CER. 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C10	CAP, CER, 10,000 PF +/-20%, 100V	407361	72982	8128-A100-W5R-103H	1		
C11	CAP, TA, 39 UF +/-20%, 20V	358234	56289	196D396X0020PE4	1		
C12	CAP, TA, 1 UF +/-20%, 35V	161919	56289	196D105X0035JA1	1		
C13	CAP, CER, 5000 PF +/-20%, 100V	175232	56289	C023B101E502M	1		
C14	CAP, CER, 12 UF +/-20%, 100V	106732	71590	CF122	2		
C15	CAP, CER, 12 UF +/-20%, 100V	106732	71590	CF122	REF		
C16	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C17	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C18	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C19	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C20	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C21	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C22	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C23	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C24	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C25	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C26	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C27	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C28	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C29	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C30	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C31	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C32	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C33	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C34	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C35	CAP, CER, 2.2 UF GMV, 25V	161927	56289	196D225X0025KA1	REF		
C36	CAP, TA, 330 UF +/-10%, 6V	193011	56289	196D331X0006KA1	1		
C37	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C38	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C39	CAP, MICA, 3300 PF, +/-1%, 500V	226175	72136	DM19F3300F	1		
C40	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
C41	CAP, TA, 10 UF +/-20%, 20V	330662	56289	196D106X0020KA1	REF		
CR1	DIODE, RCTFR BRIDGE, 2A, 100V	296509	51605	2FB200	2		
CR2	DIODE, RCTFR BRIDGE, 2A, 100V	296509	51605	2FB200	REF		
CR3	DIODE, SWITCH	203323	07910	1N4448	2		
CR4	DIODE, SWITCH	203323	07910	1N4448	REF		
CR5	DIODE, GE, 80 MA, 100 PIV	149187	22767	1N270	3		

Table 5-2. A1 Main PCB Assembly (cont)

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
CR6	DIODE, GE, 80 MA, 100 PIV	149187	22767	1N270	REF		
CR7	DIODE, GE, 80 MA, 100 PIV	149187	22767	1N270	REF		
J2	CONTACT PINS, PCB MTNG	376418	22526	75060-001	24		
J3	CONTACT PINS, PCB MTNG	376418	22526	75060-001	REF		
L1	CHOKE, 6-TURN	320911	89536	320911	1		
P1	CONN, PIN	484428	00779	9-87022-1	93		
P4	CONN, PIN	484428	00779	9-87022-1	REF		
P11	PIN, GUIDE	375840	89536	375840	1		
Q1	XSTR, SI, PNP	226290	04713	MPS3640	2	1	
Q2	XSTR, SI, PNP	369629	07263	2N5771	2	1	
Q3	XSTR, SI, PNP	369629	07263	2N5771	REF		
Q4	XSTR, SI, NPN	218396	04713	2N3904	2	1	
Q5	XSTR, SI, NPN	218396	04713	2N3904	REF		
Q6	XSTR, SI, W/INSUL KIT	325753	09214	D45CS	1	1	
Q7	XSTR, SI, PNP	195974	04713	2N3906	4		
Q8	XSTR, SI, NPN	195974	04713	2N3906	REF		
Q9	XSTR, SI, PNP	195974	04713	2N3906	REF		
Q10	XSTR, SI, PNP	195974	04713	2N3906	REF		
Q11	XSTR, SI, PNP	226290	04713	MPS3640	REF		
R1	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-45P470E	5		
R2	RES, DEP. CAR, 2.7K +/-5%, 1/4W	386490	80031	CR251-45P2K7	1		
R3	RES, DEP. CAR, 150 +/-5%, 1/4W	343442	80031	CR251-45P150E	4		
R4	RES, MTL FILM, 4.99K +/-1%, 1/8W	168252	91637	MFF1-84991F	2		
R5	RES, MTL FILM, 4.99K +/-1%, 1/8W	168252	91637	MFF1-84991F	REF		
R6	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-45P4K7	6		
R7	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-45P560E	8		
R8	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-45P560E	REF		
R9	RES, DEP. CAR, 150 +/-5%, 1/4W	343442	80031	CR251-45P150E	REF		
R10	RES, DEP. CAR, 1M +/-5%, 1/4W	348987	80031	CR251-45P1MT	1		
R11	RES, DEP. CAR, 430 +/-5%, 1/4W	441568	80031	CR251-45P430E	2		
R12	RES, DEP. CAR, 47 +/-5%, 1/4W	441592	80031	CR251-45P47E	3		
R13	RES, DEP. CAR, 47 +/-5%, 1/4W	441592	80031	CR251-45P47E	REF		
R14	RES, DEP. CAR, 47 +/-5%, 1/4W	441592	80031	CR251-45P47E	REF		
R15	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-45P560E	REF		
R16	RES, DEP. CAR, 150 +/-5%, 1/4W	343442	80031	CR251-45P150E	REF		
R17	RES, DEP. CAR, 430 +/-5%, 1/4W	441568	80031	CR251-45P430E	REF		
R18	RES, DEP. CAR, 150 +/-5%, 1/4W	343442	80031	CR251-45P150E	REF		
R19	RES, DEP. CAR, 20K +/-5%, 1/4W	441477	80031	CR251-45P20K	3		
R20	RES, DEP. CAR, 20K +/-5%, 1/4W	441477	80031	CR251-45P20K	REF		
R21	RES, DEP. CAR, 20K +/-5%, 1/4W	441477	80031	CR251-45P20K	REF		
R22	RES, DEP. CAR, 270 +/-5%, 1/4W	348789	80031	CR251-45P270E	1		
R23	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-45P4K7	REF		
R24	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-45P560E	REF		
R26	RES, VAR, 10K +/-20%, 150V	369553	54869	PT10V-10K	2	1	
R28	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-45P560E	REF		
R30	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-45P10K	1		
R31	RES, DEP. CAR, 510 +/-5%, 1/4W	441600	80031	CR251-45P510E	1		
R32	RES, DEP. CAR, SELECTED VALUE R32 MATCHED WITH A3 SIGNAL CONDITIONER	368779	89536	368779	2		
R33	RES, DEP. CAR, 4.7 +/-2%, 1/4W	342683	80031	CR251-42P4E7	1		

Table 5-2. A1 Main PCB Assembly (cont)

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
R34	RES, VAR, 10K +/-20%, 150V	369553	54869	PT10V-10K	REF		
R35	RES, DEP. CAR, SELECTED VALUE R35 MATCHED WITH A4 SIGNAL CONDITIONER	368779	89536	368779	REF		
R36	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-45P4K7	REF		
R37	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-45P470E	REF		
R38	RES, DEP. CAR, 1.8K +/-5%, 1/4W	441444	80031	CR251-45P1K8	1		
R39	RES, DEP. CAR, 180 +/-5%, 1/4W	441436	80031	CR251-45P180E	1		
R40	RES, DEP. CAR, 100 +/-5%, 1/4W	348771	80031	CR251-45P100E	1		
R41	RES, DEP. CAR, 22 +/-5%, 1/4W	381145	80031	CR251-45P22E	1		
R42	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-45P470E	REF		
R43	RES, DEP. CAR, 330 +/-5%, 1/4W	368720	80031	CR251-45P330E	1		
R44	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-45P4K7	REF		
R45	RES, DEP. CAR, 1.3 +/-5%, 1/4W	442012	80031	CR251-451E3	1		
R46	RES, DEP. CAR, 220 +/-5%, 1/4W	342626	80031	CR251-45P220E	1		
R47	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-45P4K7	REF		
R48	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-45P560E	REF		
R49	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-45P1K	1		
R50	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-45P560E	REF		
R51	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-45P470E	REF		
R52	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-45P4K7	REF		
R53	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-45P470E	REF		
R54	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-45P560E	REF		
R55	RES, DEP. CAR, 560 +/-5%, 1/4W	385948	80031	CR251-45P560E	REF		
R56	RES, DEP. CAR, 39 +/-5%, 1/4W	340836	80031	CR251-45P39E	1		
RN1	RES, NETWORK, 4.7K +/-5%, 16-PIN	416834	89536	416834	1	1	
RN2	RES, NETWORK, 39 +/-5%, 14-PIN	412866	89536	412866	1	1	
S1	SWITCH ASSY	473991	89536	473991	1		
S2	SWITCH ASSY	473991	89536	473991	REF		
S3	SWITCH ASSY	473991	89536	473991	REF		
S4	SWITCH, SLIDE, DPDT	234278	82389	XW1649	2	1	
S5	SWITCH, SLIDE, DPDT	234278	82389	XW1649	REF		
S8	SWITCH, SLIDE, .3A, 125V	354878	95146	MSS2250R	1	1	
U1	IC, TTL, SCHOTTKY, MULTIV.	404202	01295	SN74LS221N	1	1	
U2,	IC, TTL, QUAD, 2-INPUT	393033	01295	SN74LS00J	3	1	
U3	IC, TTL, QUAD, 2-INPUT	393033	01295	SN74LS00J	REF		
U4	IC, DGTL, TIL	473835	01295	SN74S196N	1	1	
U5	IC, TTL, SCHOTTKY, J-K, E-T, F/F	363440	01295	SN74S112N	1	1	
U6	IC, TTL, AND/OR INVERT W/TP GATE, 2-IN.	495473	01295	SN74S51	1	1	
U7	IC, TTL, LO-POW, SCHOTTKY	393124	01295	SN74LS74N	1	1	
U8	IC, TTL, HEX INVERTER	393058	01295	SN74S04J	1	1	
U9	IC, TTL, COUNTER	402545	01295	SN74LS90N	1	1	
U10	IC, TTL, QUAD, 2-INPUT	393033	01295	SN74LS00J	REF		
U11	IC, SCHOTTKY, QUAD, 2-INPUT	379297	01295	SN74S86N	1	1	
U12	IC, TTL, COUNTER	473843	01295	SN74LS92N	1	1	
U13	Ⓧ IC, P-MOS, COUNTER CUSTOM	460063	89536	460063	1	1	
U14	IC, QUAD, 2-INPUT, POS/GATE	393066	01295	SN74LS08J	1	1	
U15	Ⓧ IC, 6-DECADE MOS COUNTER	473215	89536	473215	1	1	
U16	IC, DGT., MOS TO LED HEX	429506	89536	429506	2	1	
U17	IC, DGT., MOS TO LED HEX	429506	89536	429506	REF		
U19	IC, SCHMITT TRIG POS/NAND GATE W/TP OUTS	483180	01295	SN74LS13N	1	1	

Table 5-2. A1 Main PCB Assembly (cont)

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
U20	IC, TTL, COUNTER	483594	89536	483594	1		
U21	IC, TTL, MSI, DAT SEL/MU	407833	01295	SN74LS157N	1	1	
U22	Ⓟ IC, C-MOS, DECODE/DRVR	429522	89536	429522	1	1	
U24	IC, LIN, VOLT-REGULATOR	355107	12040	LM340T-5	1	1	
U25	IC, LIN, OP-AMP, EXT. COMP 8-P	363515	24355	AN301AN	1	1	
U26	IC, LIN, VOLT, REG, +/-5%, 12V	473819	04713	MC79L12ACP	1	1	
U27	IC, LIN, VOLT, REG, +/-10%, 12V	408138	04713	MC78L12ACP	1	1	
U28	IC, TTL, DUAL-D, EDG/TRIG, F/F	418269	01295	SN74S74N	1	1	
U29	Ⓟ IC, C-MOS, 8-INPUT, NOR GATE, 14-PIN	408781	18725	CD4078BE	1	1	
U30	IC, ECL, QUAD, 2-INPUT NOR GATE	504431	07263	F95102	1	1	
XU13	SOCKET, IC, 40-PIN, 1A	429282	09922	DILB40P-108	2		
XU15	SOCKET, IC, 40-PIN, 1A	429282	09922	DILB40P-108	REF		
XU24	SOCKET, IC, REGULATOR	402958			1		

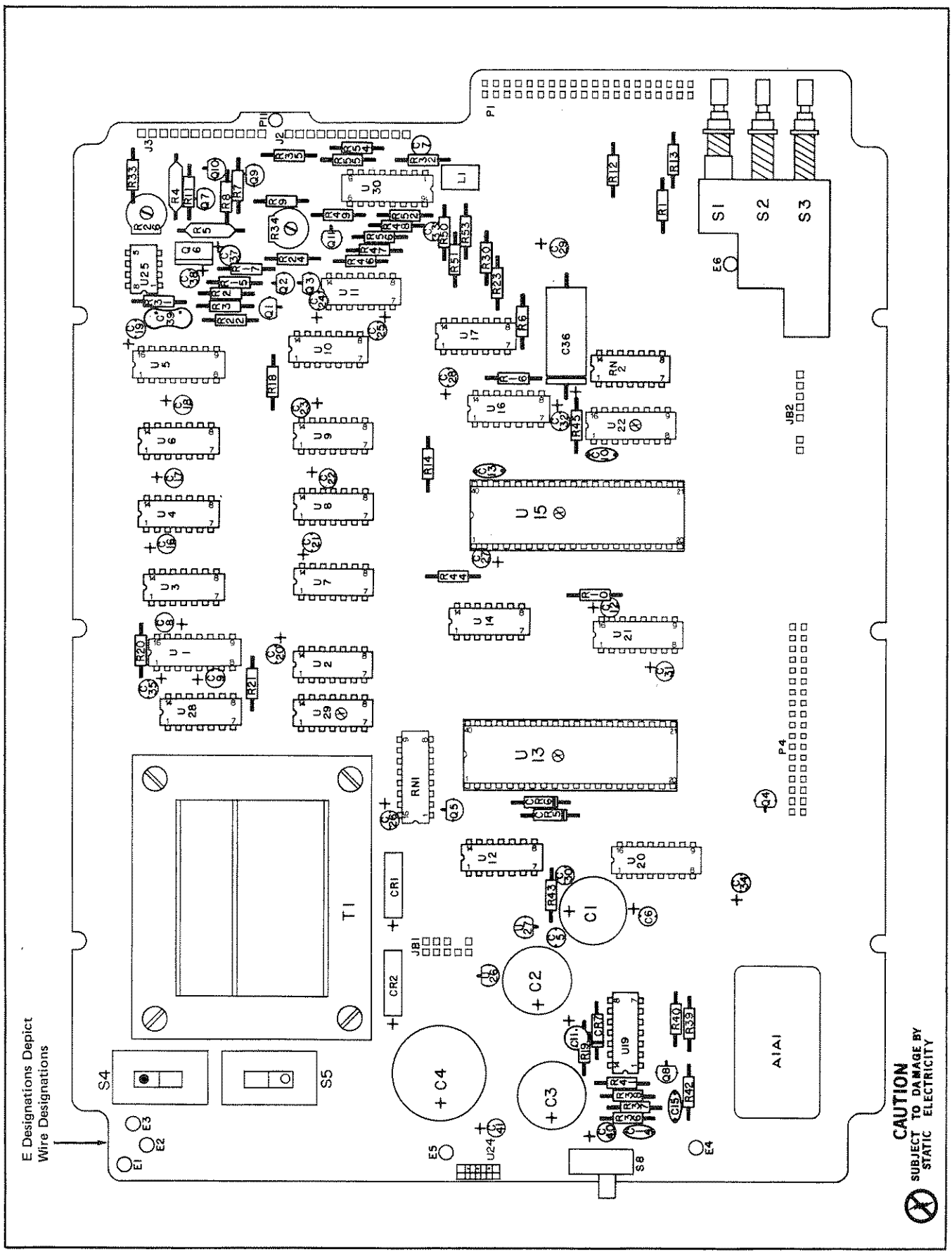


Figure 5-2. A1 Main PCB Assembly

Table 5-3. A5 Time Base PCB Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
A5	TIMEBASE PCB ASSEMBLY FIGURE 5-3 (1952B-4010T)	406918	89536	406918	REF		
C1	CAP, VAR, 22 PF, 100V	369207	80031	C010KA/20E	2		
C2	CAP, VAR, 22 PF, 100V	369207	80031	C010KA/20E	REF		
C3	CAP, CER, 22 PF +/-20%, 1000V	369157	56289	C030B102F220M	2		
C4	CAP, CER, 22 PF +/-20%, 1000V	369157	56289	C030B102F220M	REF		
C5	CAP, CER, .01 UF +/-5%, 16V	368639	14655	HCC16103P	1		
L1	CHOKE, 6-TURN	320911	89536	320911	1		
MP1	PINS, CONTACT	376574	00779	3-87022-1	5		
Q1	XSTR, N-CHANNEL, SILICON JUNCTION	386094	01295	A5T3819/SX3819	2		
Q2	XSTR, N-CHANNEL, SILICON JUNCTION	386094	01295	A5T3819/SX3819	REF		
R1	RES, COMP, 1M +/-10%, 1/8W	435008	01121	BB1051	1		
R2	RES, COMP, 1K +/-10%, 1/8W	153916	01121	BB1021	3		
R3	RES, COMP, 1K +/-10%, 1/8W	153916	01121	BB1021	REF		
R4	RES, COMP, 1K +/-10%, 1/8W	153916	01121	BB1021	REF		
Y1	CRYSTAL, QUARTZ	385732	89536	385732	1		

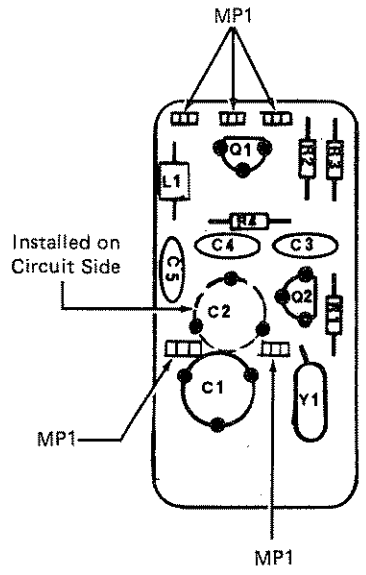
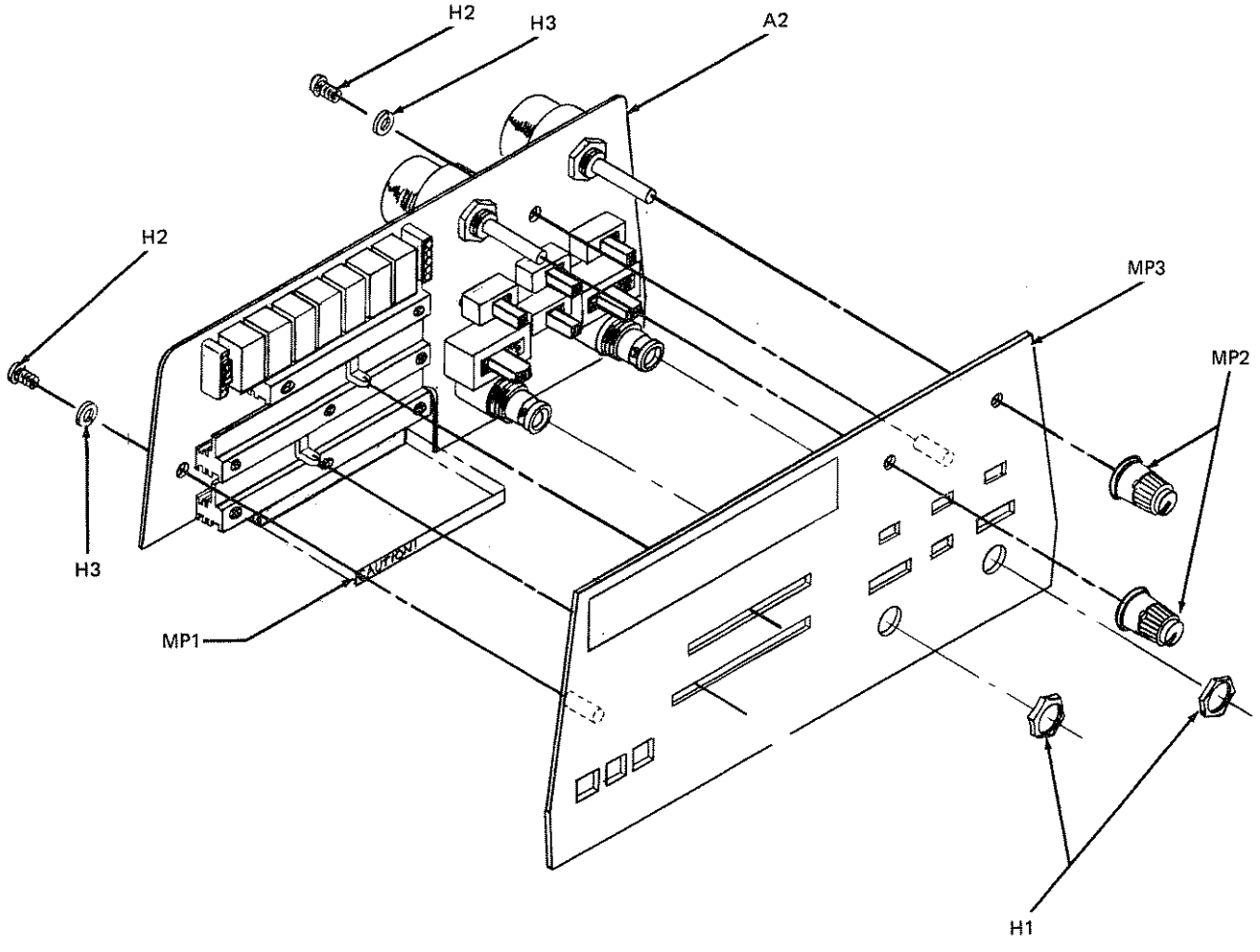


Table 5-3. A5 Time Base PCB Assembly

Table 5-4. Front Panel Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	FRONT PANEL ASSEMBLY FIGURE 5-4 (7250A-5001)						
A2	FRONT PANEL PCB ASSEMBLY FIGURE 5-5 (7250A-4002)	476655	89536	476655	1		
H1	NUT, HEX, 5/8	110916	89536	110916	2		
H2	SCREW, PHP, 4-40 X 1/2	152132	73734	19026	8		
H3	WASHER, SPLIT-LOCK #4	110395	89536	110395	2		
MP1	DECAL, FUSE CAUTION	487330	89536	487330	1		
MP2	KNOB ASSEMBLY	490755	89536	490755	2		
MP3	PANEL, FRONT	483008	89536	483008	1		



Sheet 1 of 2

Figure 5-4. Front Panel Assembly

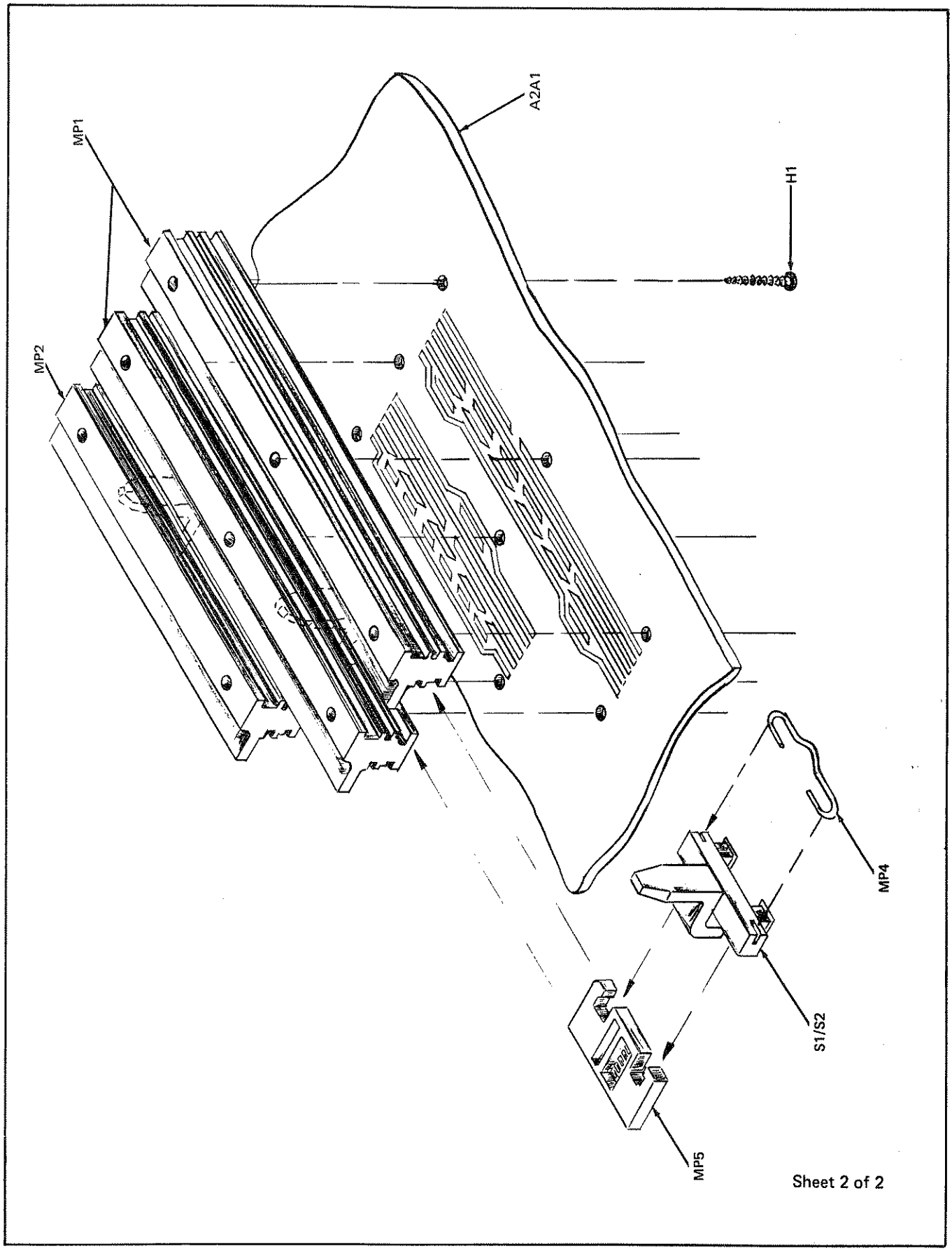


Table 5-4. Front Panel Assembly (cont)

Table 5-5. A2 Front Panel PCB Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
A2	FRONT PANEL PCB ASSY FIGURE 5-5 (7250A-4002T)	476655	89536	476655	REF		
C1	CAP, POLY, 0.068 UF +/-20%, 250V	478651	80031	C281A/AE68K	2		
C2	CAP, POLY, 0.068 UF +/-20%, 250V	478651	80031	C281A/AE68K	REF		
C3	CAP, CER, 4.7 PF +/-0.25 PF, 100V	362772	72982	8101-A100-C0G-479G-2	2		
C4	CAP, CER, 4.7 PF +/-0.25 PF, 100V	362772	72982	8101-A100-C0G-479G-2	REF		
DS1	LED, DISPLAY, RED	477562	89536	477562	7	2	
DS2	LED, DISPLAY, RED	477562	89536	477562	REF		
DS3	LED, DISPLAY, RED	477562	89536	477562	REF		
DS4	LED, DISPLAY, RED	477562	89536	477562	REF		
DS5	LED, DISPLAY, RED	477562	89536	477562	REF		
DS6	LED, DISPLAY, RED	477562	89536	477562	REF		
DS7	LED, DISPLAY, RED	477562	89536	477562	REF		
DS8	LED, IC, STRIP	483420	28480	HLMP6203	1	1	
DS9	LED, IC, STRIP	483420	28480	HLMP6203	REF		
DS10	LED ARRAY STRIP	483412	28480	HLMP6205	1		
DS11	LED ARRAY STRIP	483412	28480	HLMP6205	REF		
DS12	LED ARRAY STRIP	483412	28480	HLMP6205	REF		
DS13	LED ARRAY STRIP	483412	28480	HLMP6205	REF		
DS14	LED ARRAY STRIP	483412	28480	HLMP6205	REF		
DS15	LED, IC, STRIP	483420	28480	HLMP6203	REF		
F1	FUSE, W/PIG-TAIL	494930	75915	212.250	2	5	
F2	FUSE, W/PIG-TAIL	494930	75915	212.250	REF		
H1	SCREW, THD FRM, #2 X .406	493957	89536	493957	8		
J1	CONNECTOR, 40-PIN	460030	00779	5182-383-4	1		
J2	CONNECTOR, COAXIAL, CHANNEL A	479162	55331	1067-000-801-1	2		
J3	CONNECTOR, COAXIAL, CHANNEL B	479162	55331	1067-000-801-1	REF		
J9	SOCKET, SIP, 10-PIN	477661	00779	583773-3	2		
J10	SOCKET, SIP, 10-PIN	477661	00779	583773-3	REF		
J11	PLUG/JACK	149112	74970	105-0753	1		
MP1	CARRIER, 10-POS.	477851	00779	435999-2	2		
MP2	CARRIER, 10-POS.	477851	00779	435999-2	REF		
MP3	CARRIER, 7-POS.	477737	00779	435999-1	1		
MP4	DETENT SPRING	472878	00779	435996	2		
MP5	WIPER GUIDE	472886	00779	435998	2		
MP6	SPACER, LED (DS8 THRU DS15)	426882	89536	426882	3		
R1	RES, DEP. CAR, 4.7K +/-5%, 1/4W	348821	80031	CR251-4-5P4K7T	1		
R2	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10KT	3		
R3	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10KT	REF		
R4	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10KT	REF		
R5	RES, DEP. CAR, 10K +/-5%, 1/4W	348839	80031	CR251-4-5P10KT	REF		
R6	RES, VAR, 25K +/-30%, 1/3W	484543	89536	484543	2		
R7	RES, DEP. CAR, 12K +/-5%, 1/4W	348847	80031	CR251-45P12K	2		
R8	RES, DEP. CAR, 20 +/-5%, 1/4W	442202	80031	CR251-45P20E	2		
R9	RES, DEP. CAR, 20 +/-5%, 1/4W	442202	80031	CR251-45P20E	REF		
R10	RES, VAR, 25K +/-30%, 1/3W	484543	89536	484543	REF		
R11	RES, DEP. CAR, 12K +/-5%, 1/4W	348847	80031	CR251-45P12K	REF		
R12	RES, DEP. CAR, 33 +/-5%, 1/4W	414524	80031	CR251-4-5P33E	2		
R13	RES, DEP. CAR, 33 +/-5%, 1/4W	414524	80031	CR251-4-5P33E	REF		
S1	SWITCH, PCB SLIDE	454371	00779	435999	2		

Table 5-5. A2 Front Panel PCB Assembly (cont)

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
S2	SWITCH, PCB SLIDE	454371	00779	435999	REF		
S3	SWITCH, SLIDE, SPDT	429332	09353	1101M2-C-Q	4	1	
S4	SWITCH, SLIDE, DP 3-POS.	495291	82389	C56313L2	2	1	
S5	SWITCH, SLIDE, SPDT	429332	09353	1101M2-C-Q	REF		
S6	SWITCH, SLIDE, DP 3-POS.	495291	82389	C56313L2	REF		
S7	SWITCH, SLIDE, SPDT	429332	09353	1101M2-C-Q	REF		
S8	SWITCH, SLIDE, SPDT	429332	09353	1101M2-C-Q	REF		

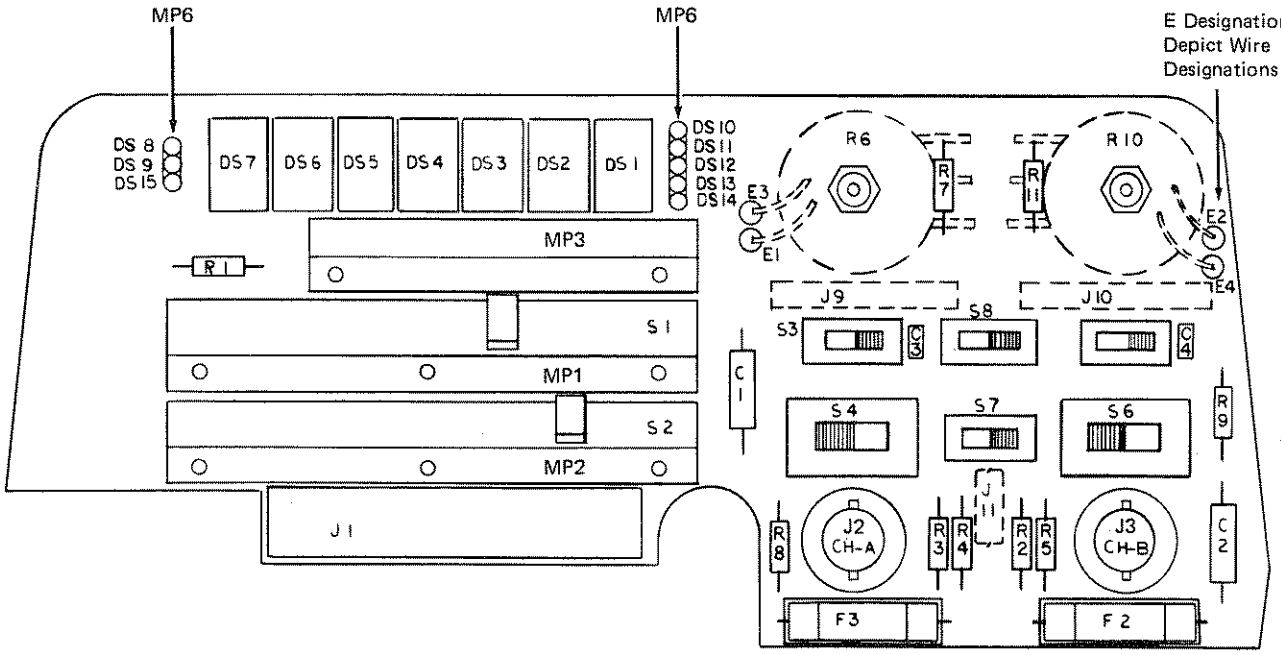


Figure 5-5. A2 Front Panel PCB Assembly

Section 6
Option & Accessory Information

TABLE OF CONTENTS

6-1. INTRODUCTION

6-2. This section of the manual contains information pertaining to the options and accessories available for the 7250A. Where applicable, these descriptions will cover the same range of information as provided in Sections 1-5 of this manual (specifications, installation, theory of operation, etc.). Schematic diagrams for any appropriate option or accessory will be found in Section 3.

6-3. Accessory information can be identified with "600-" paragraph numbers. For options, relevant paragraphs will contain the option number preceded by "6".

Accessories

600-1. GENERAL

600-2. The Table of Contents contains a list of accessories available for use with the 7250A Universal Counter/Timer. The following paragraphs contain descriptions for each type of accessory. Use the accessory model number when ordering.

600-3. Mounting Kits

600-4. Mounting kits suited for the C-size case used with the 7250A are available for standard 19-inch rack or panel format. Each kit comes complete with all mounting hardware. Model Y2014A provides for mounting a single case (size "C") in a 19-inch rack. Model Y2015 mounts two cases ("C") in a 19-inch rack. Model Y2020 mounts a single "C" case in a panel arrangement.

600-5. Instrument Cables

600-6. Two instrument ribbon cables are available for connecting the Data I/O Unit (Option -521) to the Interface PCB Assembly (Option -522), mounted in the 1120A IEEE-488 Translator. The cables, while identical in function, are available in lengths of two feet (Y7203) or five feet (Y7204). The Y7203 cable is supplied with Options -521 or -529 and Option Kits -521K or -529K.

600-7. Filter/Attenuator

600-8. The Model Y7201, as shown in Figure 600-1 is a combination variable attenuator and selectable low-pass filter intended for use as an input signal noise suppressor for Fluke counters. It features a continuously variable X5 to X100 attenuator and a set of three switch-selectable frequency filters; DC to 1 kHz, DC to 20 kHz, or DC to 100 kHz. The Y7201 allows a maximum input signal of 230V ac at 50 Hz for 30 seconds. A BNC connector is provided for convenient attachment to the counter input, and a set of 0.75" spaced banana jacks serve as the input signal connections.

600-9. In operation, the Y7201 attenuates and/or filters unwanted noise/transients from the input signal. These capabilities isolate the counter from the noise levels and, thereby, lessen the possibility of measurement errors.

600-10. To operate the Y7201, use the following procedure:

1. Connect the Y7201 to the CHANNEL A (or CHANNEL B) input to the counter.

2. Select the filter position with the lowest 3 dB point (1 kHz, 20 kHz or 100 kHz) that will accomodate the signal being measured.

3. Turn the ATTEN control fully clockwise (for maximum attenuation).

4. Connect the signal to be measured to the Y7201's banana jacks.

5. Decrease attenuation until a stable display is seen on the counter.

NOTE

For signals that are particularly noisy (or greater than 100 V p-p), it may be necessary to add more attenuation and filtering. This operation can be accomplished by adding another Y7201 in series or by adjusting the counter's attenuation and filter controls.

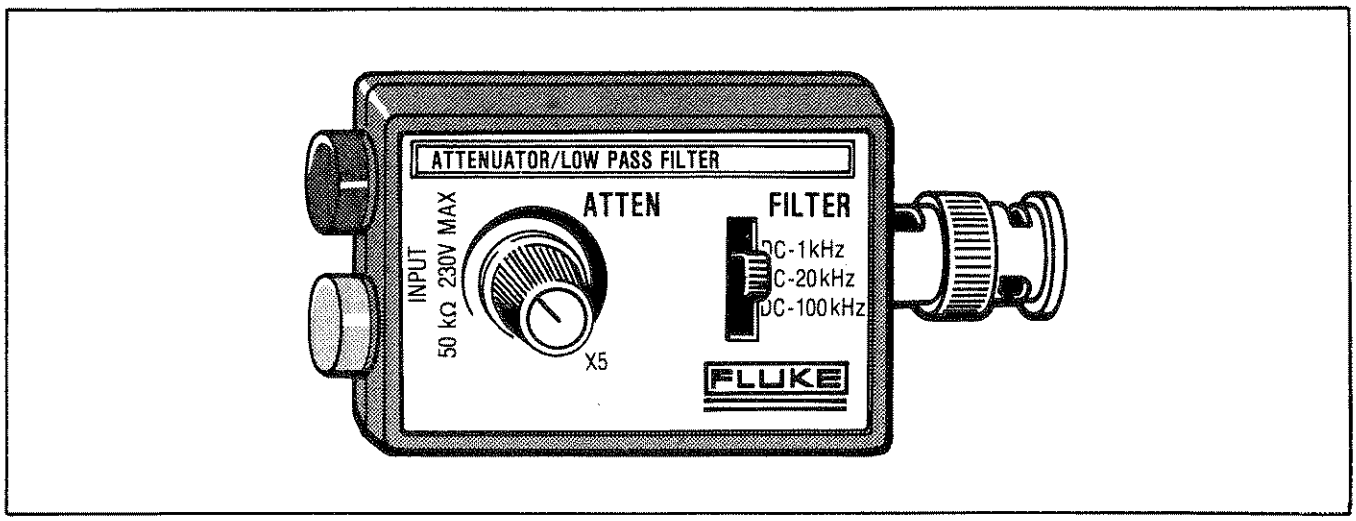


Figure 600-1. Y7201 Filter/Attenuator

Option -010
Battery Pack

6010-1. INTRODUCTION

6010-2. Option -010 is a nickel-cadmium rechargeable battery unit. The option uses "F" cell nicad batteries for a total capacity of 5.6 amp hours. With a completely discharged battery, charge time is a minimum of 16 hours at room temperature. A discharge cut-off relay has been incorporated to guard against discharging the nicads to too low a level. A thermistor sensor circuit monitors battery temperature and halts the charging if the battery gets too hot. The battery output is fused to protect it against short circuits. Housed in a separate plastic box to eliminate acid corrosion problems, the battery assembly is attached inside the top cover. This option can be installed in the field. Order kit number 72XXA-010K.

6010-3. SPECIFICATIONS

6010-4. Specifications for the -010 Battery Option are listed in Table 6010-1.

6010-5. INSTALLATION

6010-6. Use the following procedure to install the -010 Battery Option. Refer to Figure 6010-1 for installation instructions. Component location can also be determined using Figures 6010-3 and 6010-4.

1. Remove line power from the instrument.

2. Remove the top cover using the procedure described in Section 4.

3. Place the battery assembly so that the battery and Battery Option PCB are closer to the front of the instrument and the two instrument handle hold-down bolts are through the corresponding holes on the battery bracket.

4. Place the two nuts on the instrument handle hold-down bolts and tighten.

5. Remove the bottom cover using the procedure described in Section 4. Do not remove the Front or Rear Panel assemblies from the Main PCB.

6. Locate solder bridge SB1 near the BTRY/LINE switch on the bottom of the Main PCB. Remove the short. In addition, remove the short on SB6 for the 7261A only.

7. Install the bottom cover.

8. Plug the two cables from the Battery Option PCB into their appropriate connectors on the Main PCB. Grey plug to JB1, black plug to JB2.

9. Fasten the grey ribbon cable under the grey retaining clip (located on the bottom side of the instrument's top cover).

10. Install the top cover of the instrument.

Table 6010-1. Specifications

Capacity	5.6 Ampere hours
Battery Type . . .	Four size "F" nicad cells
Charge Time . . .	16 hours minimum at room temperature
Charge Protection .	Thermistor actuated shut down of charging circuit if battery gets near 65°C
Discharge Protection	Low voltage automatic shut down at about +4V to prevent battery discharging to a reversed cell condition.

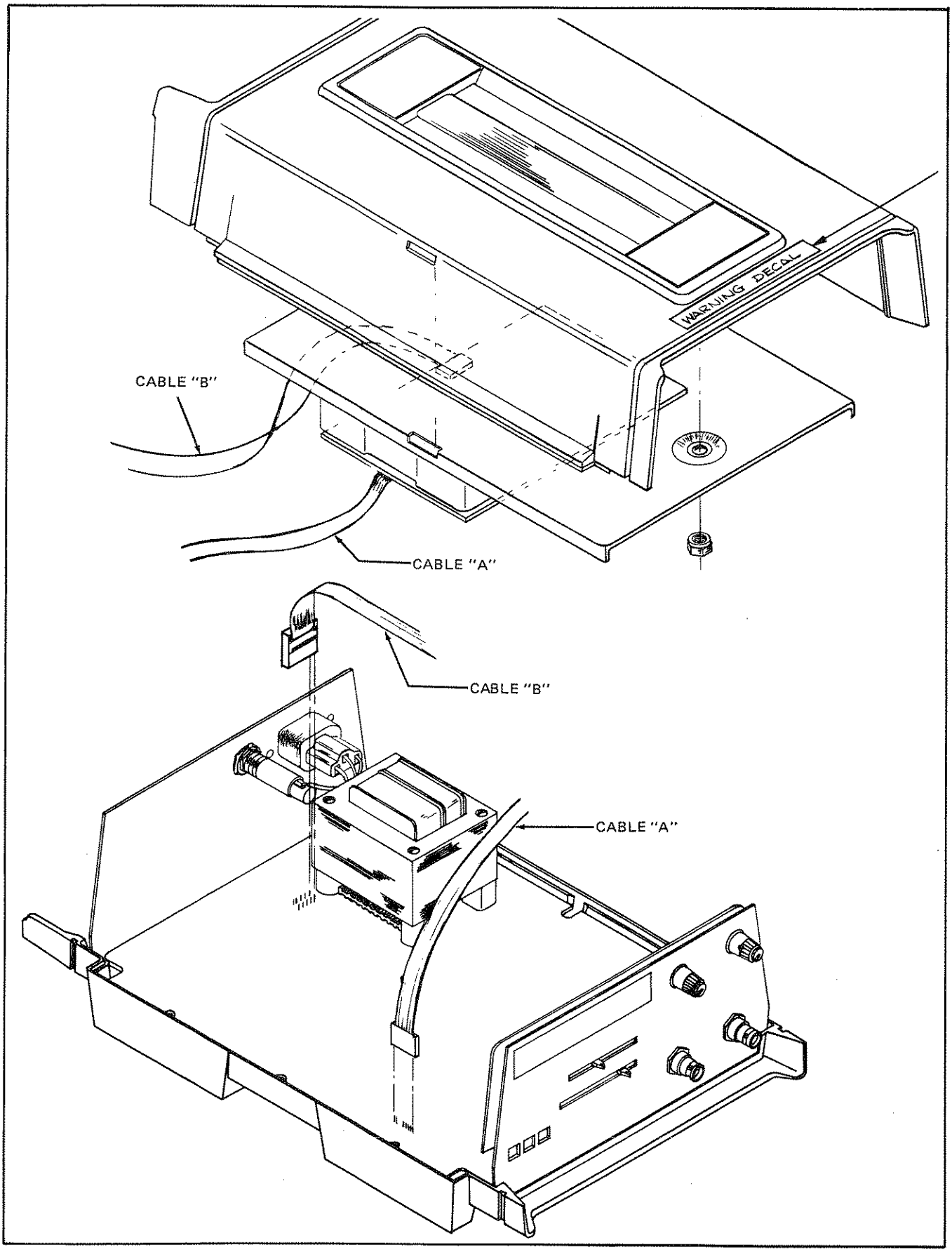


Figure 6010-1. Installation

6010-7. OPERATION

6010-8. To use the battery for instrument power, set the BTRY/LINE switch to the BTRY position. The ON/STBY switch functions normally. The instrument may be powered from the battery with the line cord plugged into line power. This serves no useful purpose, however, and discharges the battery needlessly. When the battery has discharged to about 4V, the low battery voltage relay will remove the instrument load from the battery output, preventing the battery from discharging to too low a level. Place the two POWER switches in the STBY and LINE positions to recharge the battery. After the battery has been charged sufficiently, the RESET switch on the instrument front panel must be pressed to unlatch the low voltage relay and restore normal battery operation.

6010-9. If neither oven time base option is installed, the battery will recharge any time the instrument is connected to line power and the power control is set to STBY. The charge rate is maximum when the ON/STBY switch is in the STBY position, and the BTRY/LINE switch is in the LINE position. If the battery is discharged completely, this charge rate will recharge the battery in 16 hours at temperatures around 22°C (72°F). If either oven time base is installed, the BTRY/LINE switch determines which source will power the oven. For maximum charge, the switch must be in the LINE position and the ON/STBY switch must be in the STBY position. If the BTRY/LINE switch is in the BTRY position and the ON/STBY switch is in the STBY position, the oven will draw about 200 mA of the 560 mA charging current. Under these conditions, the battery may not charge completely. If the POWER switches are in the ON and LINE positions, the charging rate will be reduced to prevent overheating inside the instrument. This charge rate is insufficient to recharge the battery but will maintain a float charge on the battery. The thermocouple sensor will halt the charge to keep the battery temperature from exceeding 65°C (149°F). (This will only occur in high ambient temperature environments.) The battery charge will automatically resume when the battery has cooled enough.

NOTE

Battery manufacturers recommend that nicad batteries should not be stored for extended periods of time without recharging at least every 90 days. Storage temperature below 25° C (77° F) is recommended.

6010-10. THEORY OF OPERATION

6010-11. The theory of operation for the -010 Option will be divided into a basic functional description of the major circuits of the option and a detailed circuit analysis of each circuit.

6010-12. BASIC FUNCTIONAL DESCRIPTION

6010-13. As Figure 6010-2 shows, there are four main sections to the Battery Option PCB circuitry. The Current Source uses +5V unregulated power from the Main PCB to provide the charging current for the battery. The charging rate (high or low) is determined by the position of the ON/STBY switch. The Battery Hi-Temp Circuit reduces the charging current if the battery temperature approaches 65°C. The Low Battery Voltage Relay circuit normally passes the battery power on to the BTRY/LINE switch. Should the battery voltage drop to around 4V, the relay contacts will open, removing the load from the battery. The RESET switch on the instrument front panel must be pressed to restore the Low Battery Voltage Relay Circuit. If the BTRY/LINE switch is in the BTRY position, the +5V power from the battery is connected to the ON/STBY switch, and the oven if an oven time base is installed. If the ON/STBY switch is in the ON position, the battery power is supplied to the instrument and the Inverter circuit. The Inverter circuit provides operating voltages for the -5V, +12V and -12V regulators.

6010-14. DETAILED CIRCUIT ANALYSIS

6010-15. The Battery Option Schematic in Section 8 will be used to illustrate the detailed circuit analysis. The battery and thermistor are located inside the battery case.

6010-16. Battery Hi-Temp Circuit

6010-17. The Battery Hi-Temp Circuit is an inverting amplifier that protects the battery by reducing the battery charging current as the battery temperature approaches 65°C. It does this by altering the bias voltage of the Current Source controller to turn off the current source. The inverting amplifier is U1B with thermistor RT1 used as the feedback resistor. The positive input of the op amp is COMMON. The negative input is the -12V coupled through R9. RT1 is located next to the battery. When the battery is about 22°C, the resistance of RT1 will be about 50Ω. At this time, the output of the inverting amplifier (felt at the lower junction of R7 and R8) is about +.4V. RT1 exhibits a positive temperature coefficient. As the battery temperature rises, the resistance of RT1 increases. When the battery temperature approaches 65°C, the resistance of RT1 passes over a sharp knee and approaches 500Ω. The output of the negative gain amplifier approaches +5V.

6010-18. Current Source

6010-19. The Current Source uses the unregulated +5V from the Main PCB to provide charging current for the

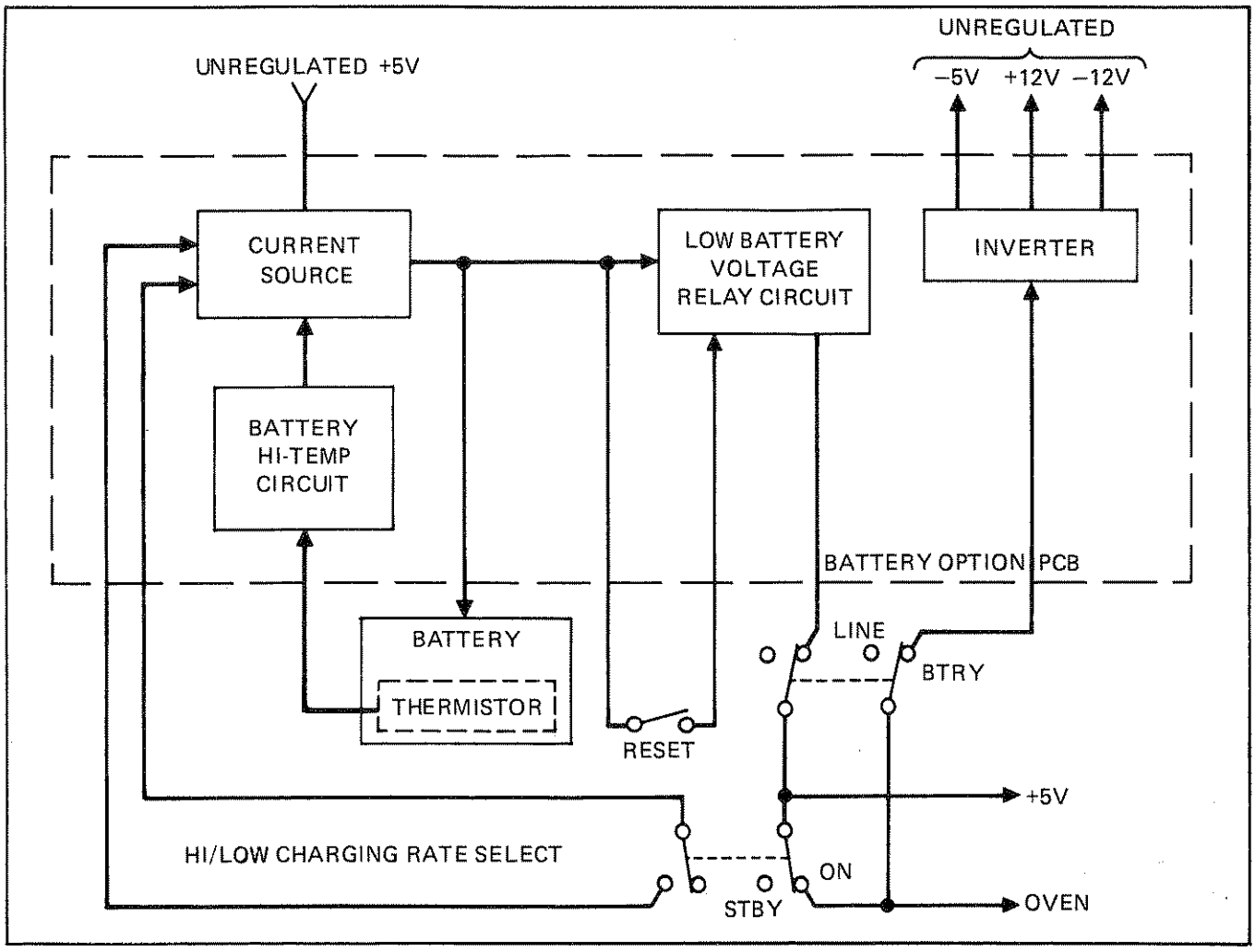


Figure 6010-2. -010 Option Block Diagram

battery. This circuit consists of the series pass element, Q1; the sensing element, R1; the control element, U1A; and their associated circuitry. Q1 directly controls the current charging the battery. The base bias of Q1 is in turn controlled by the output of U1A. The positive input is battery voltage felt on the battery side of R1 (TP2). The negative input is picked off the voltage divider network composed of R2, R8 and sometimes R7. The voltage divider is between the input side of R1 (TP1) and the output of the Battery Hi-Temp circuit.

6010-20. The charging current is changed by altering the input to U1A from the voltage divider. The voltage divided input is altered by changing the position of the ON/STBY switch. When the switch is in the STBY position, R7 is placed in parallel with R8. Their combined resistance is about one-fifth that of R8 alone. At normal operating temperatures, the bottom of the voltage divider is at +0.5V and the top is at battery voltage plus the voltage drop across R1. The op amp causes Q1 to pass nominally 560 mA through R1. If the ON/STBY switch is in the ON position, R7 is no longer in parallel with R8. This change in the voltage divider input to U1A will cause the charging current to decrease to nominally 110 mA. If the battery temperature approaches 65° C, the bottom of the voltage divider becomes +5V and the voltage at TP1 approaches the battery voltage. This decreases the output of the op amp cutting off Q1. As the battery cools, the resistance of the thermistor decreases allowing the battery charge to resume. If F1 blows, removing the regulated input to U1A, CR10 will limit the conduction of Q1 so that the voltage at TP2 does not exceed 6V.

6010-21. Low Battery Voltage Relay Circuit

6010-22. The low battery voltage relay keeps the battery from discharging to a reversed cell condition by removing the battery load when battery voltage drops to about 4V. The battery is connected to its load through K1, a two coil latching relay. During normal operation, the battery and its load are connected, Q2 and Q6 are off and Q5 is in saturation. When battery voltage drops to about 4V, the base bias on Q5 (TP5) is low enough to cut Q5 off. This lets the input on pin 13 of flip-flop U2 rise. This will

change the state of U2 making the output on pin 11 of U2 go low. This causes Q6 to conduct, charging C2 and turning Q2 on. When Q2 conducts, the coil of K1 in the collector of Q2 will energize, opening K1. When K1 removes the battery loads, the input circuitry for Q2 is deenergized. C2 has been charged to make Q2 conduct long enough to insure that K1 is latched in the open condition. After the battery has been recharged, pressing the RESET switch on the front panel will connect battery voltage to both the reset coil of K1 and pin 6 of U2. The RESET switch contacts will be closed long enough to insure that K1 will be latched shut. This will restore the connection between the battery and its load. Q5 will go into saturation. The battery voltage at pin 6 of U2 will cause pin 11 to go high, turning off Q6.

6010-23. Inverter

6010-24. The Inverter is composed of Q3, Q4, T1 and their associated circuitry. The three components form an oscillator that runs at about 15 kHz. This oscillation allows T1 to step up the battery voltage to provide rectified operating voltages to the -5V, +12V and -12V regulators for instrument power.

6010-25. PERFORMANCE TEST

6010-26. Use the following procedure as a performance test. Table 6010-2 lists the test points. The component location diagram at the end of this option can be used to locate these test points. The instrument will be referred to as the UUT (Unit Under Test). Use a variable DC power supply with an output range of at least 3-5V and the test equipment listed in Section 4.

1. Remove the top cover of the UUT using the procedure given in Section 4. Leave the cables from the Battery Option PCB connected to the Main PCB and lay the top cover beside the instrument, upside-down. The grey ribbon cable will have to be removed from the retaining clip on the bottom side of the top cover.

Table 6010-2. Test Points

TEST POINTS	COMMENTS
TP1, TP2	Voltage across sensing resistor, R1.
TP3	COMMON
TP4	Battery voltage.
TP5	Low Battery Voltage Sensing Point
TP6	Low Battery Voltage Cut-Off Signal.

2. Connect the UUT to line power.

3. On the UUT front panel:

   a. Set the ON/STBY switch to the STBY position.

   b. Set the BTRY/LINE switch to the LINE position.

4. Connect the DVM: + to TP2, - to TP3.

5. Verify that the DVM reads greater than 5V. If it does not, continue the charge until this reading (Battery Voltage) is at least 5V.

NOTE

In the next step, the DVM test leads must be isolated from ground.

6. Connect the DVM: + to TP1, - to TP2.

7. Verify that the DVM reads between 96 mV and 128 mV.

8. Set the ON/STBY switch to ON.

9. Verify that the DVM reads between 14 mV and 30 mV.

10. Set the ON/STBY switch to STBY.

11. Connect the DVM: + to TP4, - to TP3.

12. Verify that the DVM reads battery voltage. If there is no voltage present, press the RESET switch on the front panel. The DVM should now read battery voltage.

CAUTION

The 7260A must be disconnected from ground during the following soldering procedures. Disconnect the power cord and any other connection (e.g., BNC) that may be introducing a ground to the instrument. The use of an ungrounded soldering iron is recommended.

13. Unsolder an end of the fuse wire located on the PCB near the battery harness.

14. Adjust the DC Power Supply for a +5V output.

15. Connect the DC Power Supply + to TP2, - to TP3.

16. Connect the DVM + lead to TP4, – lead to ground.

17. Slowly reduce the DC Power Supply voltage until the relay opens as indicated by the voltage of TP4 dropping suddenly to 0V. (The click of the relay may also be heard.)

18. Verify that the output voltage of the DC Power Supply is between +3.8V and +4.3V.

19. Disconnect the DC Power Supply. Resolder the fuse wire.

20. On the front panel of the UUT:

a. Press and release the RESET switch.

b. Set the ON/STBY switch to the ON position.

c. Set BTRY/LINE switch to the BTRY position.

d. Set the RESOLUTION switch to the 1 kHz position.

e. Set the function select switch to the CHK position.

21. Verify that the UUT display reads 10.000.

6010-27. MAINTENANCE

6010-28. Battery Replacement

6010-29. Use the following procedure to replace the battery:

1. Remove the line power from the instrument.

2. Remove the top cover of the instrument using the procedure given in Section 4. Place the top cover upside-down on the work surface.

3. Disconnect the two cables between the Battery PCB and the Main PCB.

4. Remove the four screws holding the battery case to the battery bracket.

5. Note the position of the thermistor. This will be important in a later step.

6. Lift the battery case and Battery Option PCB off the battery and place it to one side.

7. Unsolder the two wires connected to the battery (white and black).

8. Dispose of the old battery.

9. Solder the white and black wires to the tabs on the new battery. White to the tab on the recessed battery end (+) and black to the tab on the flush battery end (–).

10. Replace the battery case being sure to place the thermistor in the same position noted in step 5.

11. Connect the two cables between the Battery PCB and the Main PCB.

12. Replace the top cover.

6010-30. Fuse Replacement

6010-31. Use the following procedure to replace the fuse on the Battery Option PCB:

1. Remove the line power from the instrument.

2. Remove the top cover from the instrument using the procedure given in Section 4. Place the top cover upside-down on the work surface.

3. Unsolder the ends of F1 from its terminals.

4. Solder a suitable length of #35 magnet wire between the fuse terminals.

5. Place the top cover on the instrument.

6010-32. LIST OF REPLACEABLE PARTS

6010-33. Table 6010-3 is a list of replaceable parts for the battery assembly. Figure 6010-3 is the component location diagram for this table. Table 6010-4 is a list of replaceable parts for the Battery Option PCB Assembly. Figure 6010-4 is the component location diagram for this table.

Table 6010-3. Battery Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	BATTERY OPTION ASSEMBLY BATTERY ASSY PCB	OPTION	-010		1		
BT1	BATTERY ASSY	484048	89536	484048	1		
H1	SCREW, PHP, 4-40 X 1/4	129890	73734	19022	1		
H2	SCREW, PHP, 6-32 X 1/4	152140	73734	19042	8		
H3	WASHER, SPLIT #4	110395	89536	110395	1		
H4	WASHER, LK #4	185417	89536	185417	1		
H5	WASHER, #6	152140	89536	152140	4		
MP1	BRACKET, BATTERY	476200	89536	476200	1		
MP2	CASE, BATTERY	475459	89536	475459	1		
MP3	CABLE TIE	172080	06383	SST-1M	1		
MP4	INSULATOR, REG.	412809	13103	43-77-8	1		
Q1	TRANSISTOR, SI, NPN, PWR	325761	09214	D44C5	1	1	

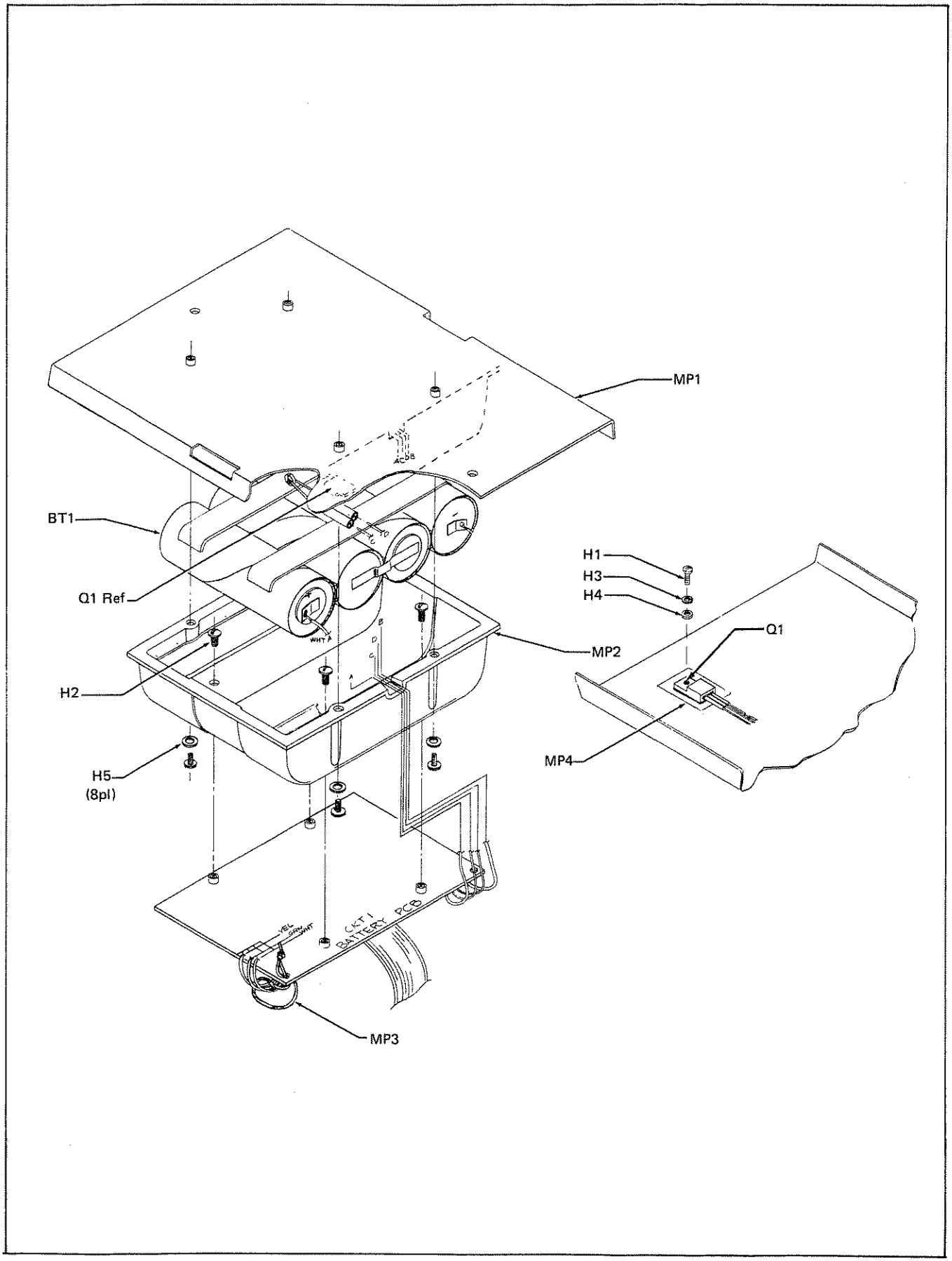


Figure 6010-3. Battery Assembly

Table 6010-4. Battery PCB Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	Ⓐ BATTERY PCB ASSY --FIGURE 6010-4 (7220A-4010T)	ORDER	NEXT	HIGHER ASSEMBLY	REF		
C1	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	6		
C2	CAP, TA, 4.7 UF +/-20%, 25V	161943	56289	196D475X0025KA1	1		
C3	CAP, TA, 330 UF, +/-10%, 6V	193011	56289	150D337X9006S	1		
C4	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C5	CAP, CER, 47 PF +/-20%, 1000V	369132	56289	C030B102H470J	1		
C6	CAP, CER, 0.1 UF +/-GVM, 25V	369199	71590	UK-25-104	1		
C7	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C8	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C9	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
C10	CAP, TA, 2.2 UF +/-20%, 20V	161927	56289	196D225X0020HA1	REF		
CR1	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	9		
CR2	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR3	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR4	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR5	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR6	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR7	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR8	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR9	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	REF		
CR10	DIODE, ZENER, 6.8V	260695	07910	1N754A	1		
H1	SCREW, RHD, PH, 4-40 X 3/8	152124	73734	18024	2		
H2	NUT, HEX, #4	147611	89536	147611	2		
H3	WASHER, LOCK #4	110403	73734	1302	2		
H4	SPACER	500074	89536	500074	4		
K1	RELAY, LATCHING	484535	89536	484535	1		
L1	CHOKE	502138	89536	502138	1		
MP1	SPACER, PCB COMPONENT	296319	89536	269319	1		
MP2	PLUG, CONNECTOR KEY	500801	52152	3435-0000	1		
Q2	XSTR, SI, NPN	346916	89536	346916	1	1	
Q3	XSTR, SI, NPN, PWR	325720	04713	MJE3055	2	1	
Q4	XSTR, SI, NPN, PWR	325720	04713	MJE3055	REF		
Q5	XSTR, SI, NPN	218396	04713	2N3904	1	1	
Q6	XSTR, SI, PNP	195974	04713	2N3906	1	1	
R1	RES, WW, 0.2 +/-3%, 0.7W	255661	89536	255661	1	1	
R2	RES, MTL. FILM, 1.1K +/-1%, 1/8W	241497	91637	CMF551101F	1		
R4	RES, DEP. CAR, 100K +/-5%, 1/4W	348920	80031	CR251-4-5P100K	1		
R5	RES, MTL. FILM, 86.6K +/-1%, 1/8W	291468	91637	CMF558661F	1		
R6	RES, DEP. CAR, 47 +/-5%, 1/4W	441592	80031	CR251-4-5P47E	2		
R7	RES, MTL. FILM, 61.9K +/-1%, 1/8W	237230	91637	CMF556191F	1		
R8	RES, MTL. FILM, 249K +/-1%, 1/8W	268805	91637	CMF552493F	1		
R9	RES, DEP. CAR, 1.2K +/-5%, 1/4W	441378	80031	CR251-4-5P1K2	1		
R10	RES, DEP. CAR, 47 +/-5%, 1/4W	441592	80031	CR251-4-5P47E	REF		
R11	RES, COMP, 10 +/-5%, 1W	166298	01121	GB1005	1		
R12	RES, DEP. CAR, 330 +/-5%, 1/4W	368720	80031	CR251-4-5P330E	1		
R13	RES, DEP. CAR, 82 +/-5%, 1/4W	442277	80031	CR251-4-5P82E	1		
R14	RES, MTL. FILM, 10K +/-1%, 1/8W	168260	91637	CMF551002F	1		
R15	RES, MTL. FILM, 6.65K +/-1%, 1/8W	294918	91637	CMF556651F	1		
R16	RES, THERMISTOR, 10K +/-10%, 3 MW	104596	15801	JA41J1			

Table 6010-4. Battery PCB Assembly (cont)

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
R17	RES, DEP. CAR, 1K +/-5%, 1/4W	343426	80031	CR251-4-5P1K	REF		
R18	RES, DEP. CAR, 470 +/-5%, 1/4W	343434	80031	CR251-4-5P470E	1		
T1	XFMR, POWER	486530	89536	486530	1		
U1	IC, LINEAR OP AMP	414284	12040	LM1458N	1	1	
U2	Ⓐ IC, COS/MOS, NOR GATES, POS LOGIC	355172	02735	CD4001AE	1	1	
W1	CABLE, BATTERY #1	488403	89536	488403	1		
W2	CABLE, BATTERY #2	488411	89536	488411	1		
W3	CABLE, BATTERY #3	491704	89536	491704	1		
XQ2	TRANSIPAD	152207	07047	10123DAB	1		

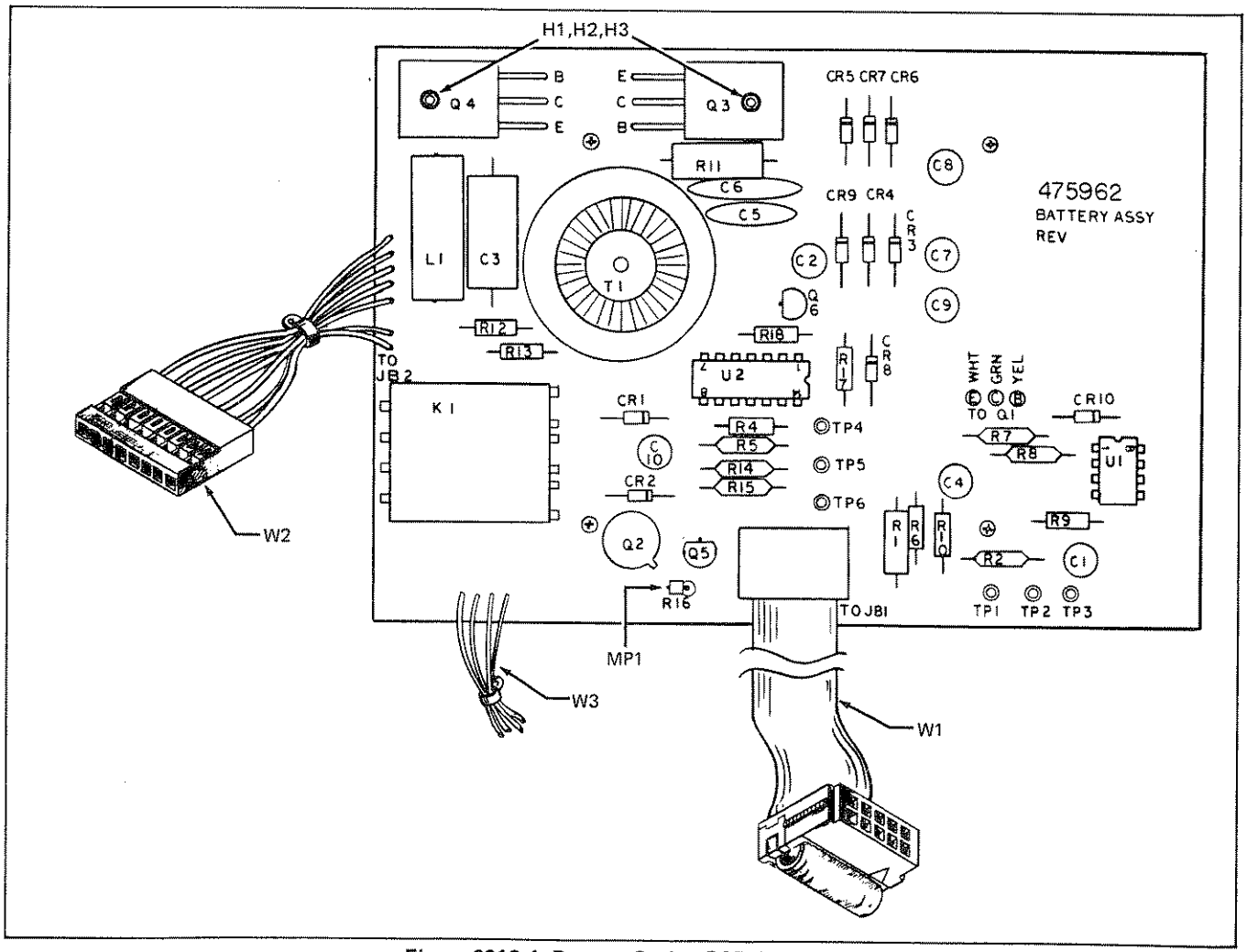


Figure 6010-4. Battery Option PCB Assembly

Option-112
2 PPM TCXO

6112-1. INTRODUCTION

6112-2. Option -112 is a temperature compensated crystal oscillator (TCXO) with an intrinsic stability greater than the standard time base. This increased stability is due to a temperature compensation network. Figure 6112-1 shows the frequency variation for change in temperature for an uncompensated oscillator and the compensation network effect. The resulting frequency deviation (solid line) is held to a minimum over the designated temperature range. If the temperature limits are exceeded, the time base stability may exceed the specified value.

6112-3. SPECIFICATIONS

6112-4. Specifications of the 72XXA-112 Option are listed in Table 6112-1. Comparative specifications for the other time bases available are listed in Section 1.

6112-5. INSTALLATION

6112-6. Installation of the 2 PPM TCXO (Option -112) necessitates removal of the counter's Main PCB; refer to disassembly instructions in Section 4. For each counter, the TCXO is installed in the left rear corner of the Main PCB. Use the following installation procedure:

1. Unsolder and remove any other time base already installed.

2. Referring to Figure 6112-2, install the TCXO and the insulator.

3. While exercising care not to overheat the multilayer Main PCB, solder the TCXO connections.

4. Complete jumper and solder bridge arrangements as illustrated in Figure 6112-2 and described below:

a. 7250A: Ensure that solder bridge SB2 is not shorted (bottom of Main PCB, left front corner). Also remove any jumper between W1 and +5V, and jumper W1 to +12V (top of Main PCB, left front corner).

b. 7260A or 7261A: If necessary, remove the shorts on solder briges SB2 (bottom of Main PCB, left front corner) and SB4 (bottom, left rear). Jumper SB5 (left rear, next to SB4) to the immediately adjacent side of SB4.

6112-7. OPERATION

6112-8. Operation of the instrument with the -112 Option installed is the same as operation of a standard instrument. Refer to Section 2 for operating instructions.

6112-9. CALIBRATION

6112-10. Calbration for the TCX0 (Option -112) time base necessitates the use of a frequency reference with an accuracy of $\pm 1 \times 10^{9}$. A cesium standard, such as the HP 5061A, is recommended. This calibration procedure calls for applying the reference frequency to Channel A and adjusting the time base for a counter display of the known input. At the 0.1 Hz RESOLUTION setting on the counter, this method yields a demonstated accuracy of 2 parts in 10^{8} ($\pm$ one count error). Proceed with the following steps:

1. Ensure that the counter's top and bottom covers are installed.

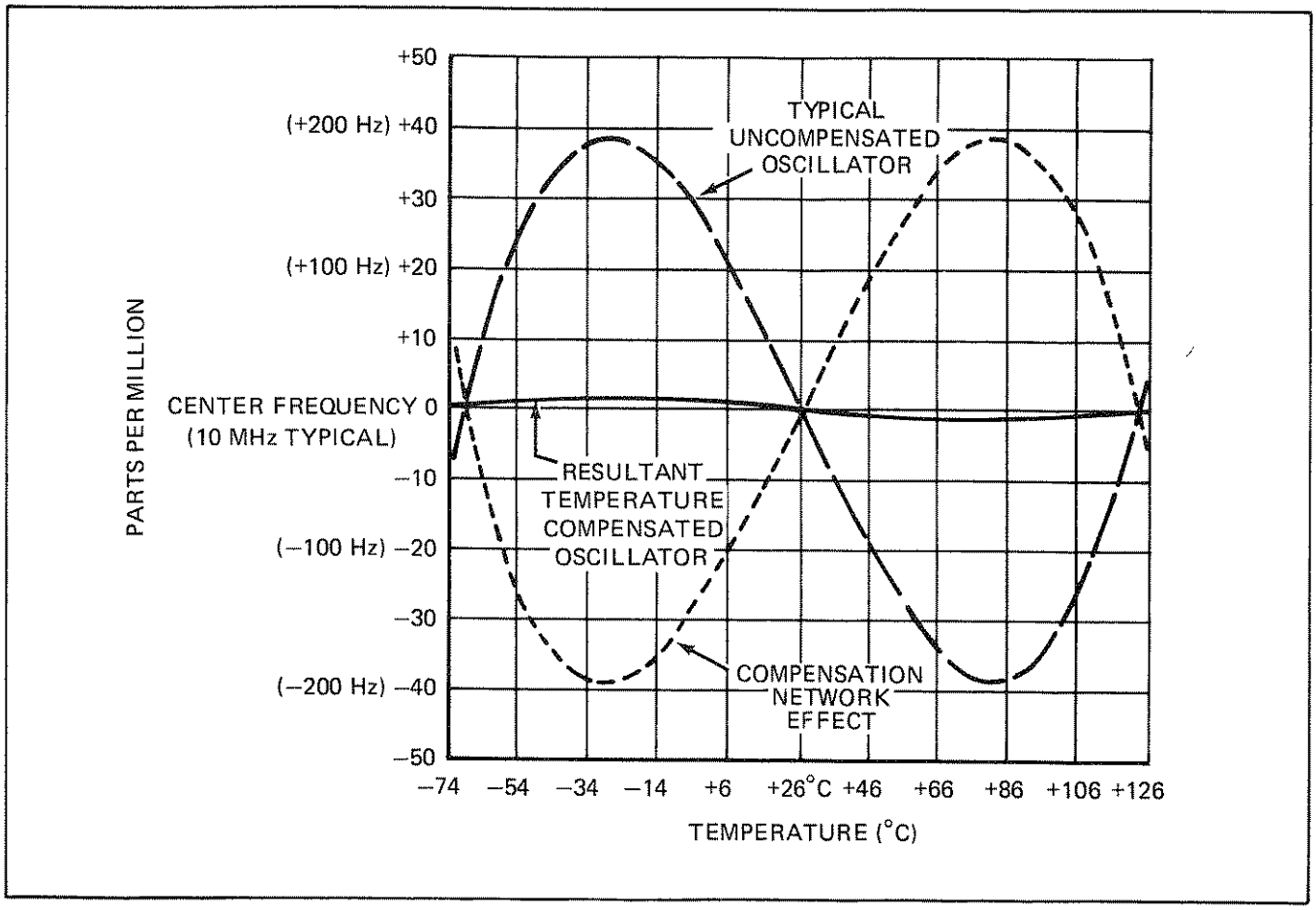


Figure 6112-1. Compensation Effects

Table 6112-1. Option 72XXA-112 Specifications

Nominal Frequency	10 MHz
Aging Rate	$\pm 3 \times 10^{-7}$/month $\pm 1 \times 10^{-6}$/year
Accuracy with Temperature (0° to 50°C) .	$\pm 2 \times 10^{-6}$
Line Voltage . . . . . (10% line variation)	$\pm 2 \times 10^{-8}$

2. Apply power to the counter and allow for a minimum warmup of 2 hours.

3. Set counter controls and connections as defined in Section 4 of this manual ("Time Base Calibration").

4. Connect the 5 MHz (100 mV) frequency reference output to CHANNEL A input on the counter.

5. If necessary, adjust the time base so that the counter's display corresponds to the first reading presented in Table 6112-2. The adjustment is accessed through a hole in the left rear corner of the bottom case half. Use a JFD 5284 (or equivalent) non-ferrous adjustment tool. If installed at the rear of the bottom case half, the bail will have to be removed to allow access.

6. Change the counter's RESOLUTION setting to the next step listed in Table 6112-2 and repeat step (5) for the respective display. Display update in the 0.1 Hz setting occurs every 10 seconds.

Table 6112-2. Calibration

RESOLUTION	DISPLAY (±1 COUNT)
1 Hz	5000.000 kHz (7250A, 7260A, 7261A) 5.000000 MHz (7220A)
0.1 Hz	000.0000 kHz* (7250A) 5000.0000 kHz (7260A, 7261A) 5.0000000 MHz (7220A)

NOTE

When the OVFL LED is illuminated, observed the GATE LED (on) to verify that a measurement is being made.

6112-11. REPLACEABLE PARTS

6112-12. The 72XXA-112 Option is a completely sealed unit containing no replacement parts. A replacement can be ordered by using Fluke Part Number 461871.

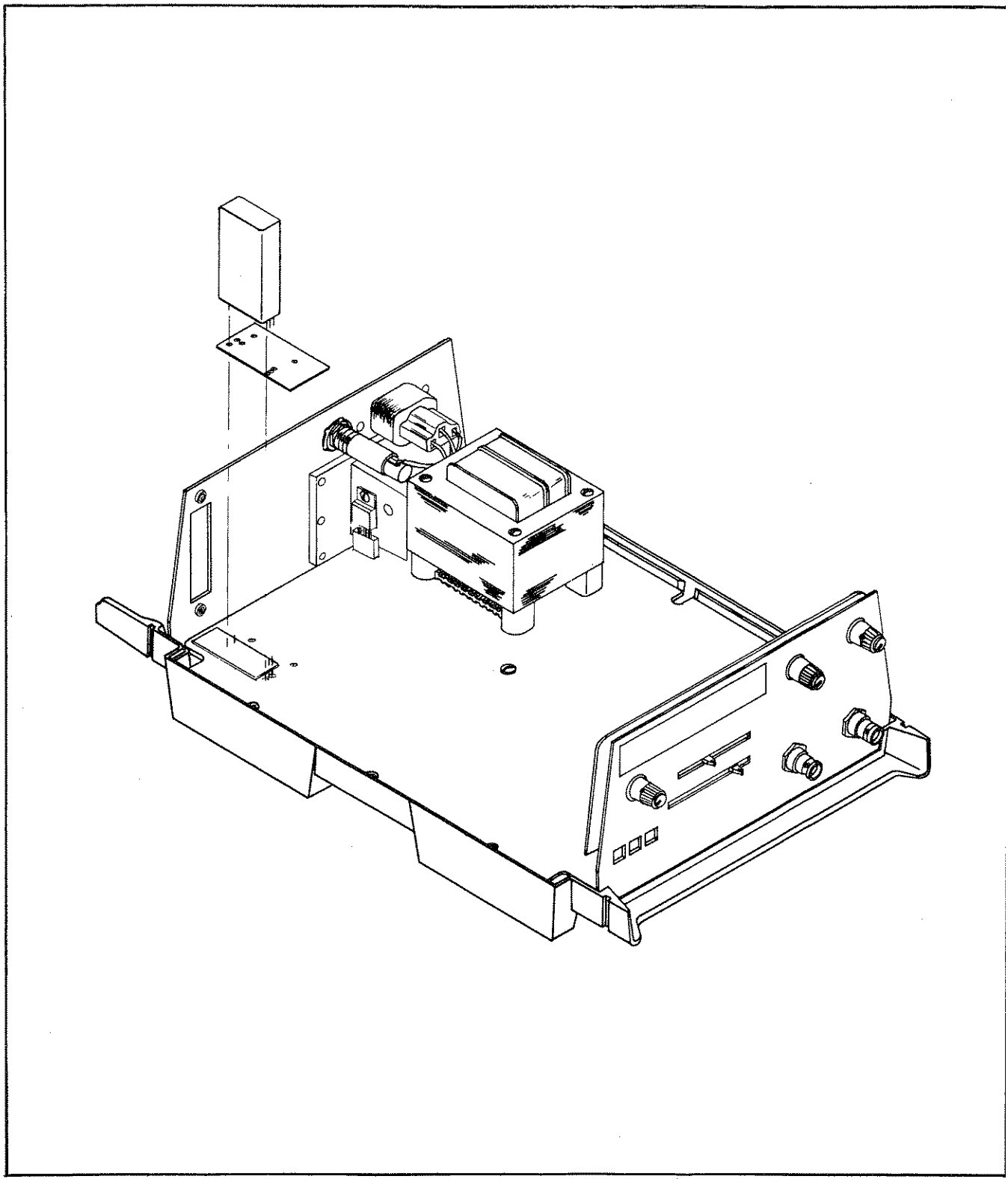


Figure 6112-2. Installation

Option-131
Low Power Oven Time Base

6131-1. INTRODUCTION

6131-2. The -131 Option is a crystal oscillator inside a temperature stabilized oven. The oven uses an extremely small amount of power. After the assembly is warmed up, power consumption is 1 watt, typically. This allows oven controlled time base accuracy with a battery powered instrument. Operation and Calibration of an instrument equipped with the -131 Option is the same as with a standard instrument. Refer to Sections 2 and 4 of this manual for additional information.

6131-3. SPECIFICATIONS

6131-4. The specifications of the -131 Option are listed in Table 6131-1.

6131-5. INSTALLATION

6131-6. Installation of the Low Power Oven Time Base (Option -131) necessitates removal of the counter's Main PCB; refer to disassembly instructions included with Section 4. For each counter, the Low Power Oven Time Base is installed in the top left rear corner of the Main PCB. Use the following installation procedure:

1. Unsolder and remove any other time base already installed.

2. Referring to Figure 6131-1, install the Low Power Oven Time Base and insulator. Use the provided hardware to secure the time base to the Main PCB.

3. While exercising care not to overheat the multilayer Main PCB, solder the time base connections.

4. Complete jumper and solder bridge arrangements on the Main PCB as illustrated in Figure 6131-1 and described below:

   a. 7220A: If necessary, remove the short at SB4 and jumper SB5 (bottom of Main PCB, left rear corner). Jumper SB2 (bottom, left front corner).

   b. 7250A: If necessary, remove the short between W1 and +12V and jumper W1 to +5V (top of Main PCB, left front corner). Jumper SB2 (bottom of Main PCB, left front corner).

   c. 7260A or 7261A: Remove the short at SB5 and jumper SB4 (bottom of Main PCB, left rear). Jumper SB2.

Table 6131-1. -131 Option Specifications

Nominal Frequency	10 MHz
Aging Rate	1×10^{-7}/month*
Accuracy with Temperature (0° to 50°C)	$\pm 1 \times 10^{-7}$
Line Voltage (10% line variation)	2×10^{-8}
Warmup**	
10 minutes	5×10^{-7}
20 minutes	3×10^{-8}

* After 5 days continuous operation.

** Specifies offset from final frequency value (the value after 24 hours).

6131-7. CALIBRATION

6131-8. Calibration for the Low Power Oven Time Base necessitates the use of a frequency reference with an accuracy of $\pm 1 \times 10^{-9}$. A cesium standard, such as the HP

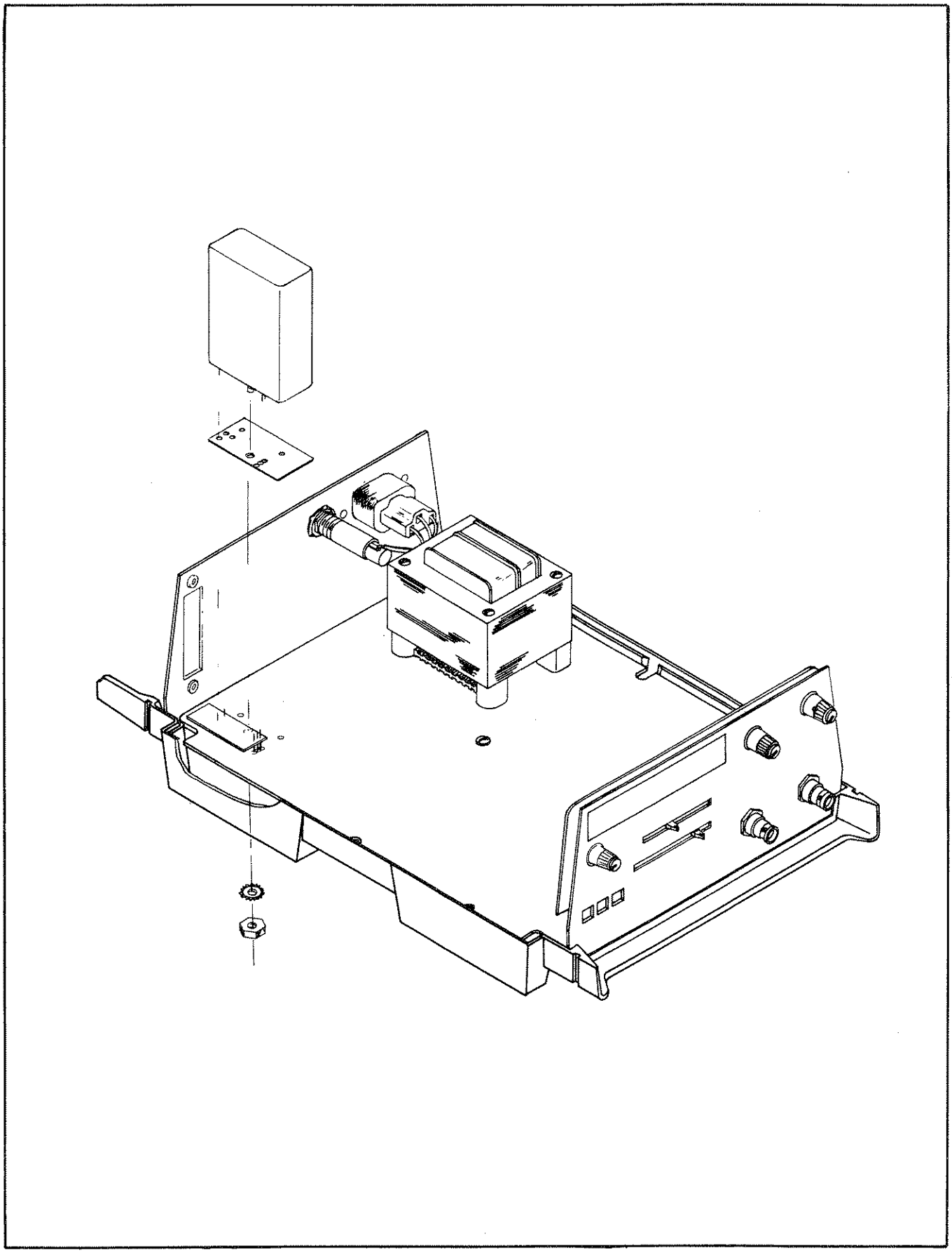


Figure 6131-2. Installation

5061A, is recommended. This calibration procedure calls for applying the reference frequency to Channel A and adjusting the time base for a counter display of the known input. At the 0.1 Hz RESOLUTION setting on the counter, this method yields a demonstrated accuracy of 2 parts in 10^8 (± one count error). Proceed with the following steps:

1. Ensure that the counter's top and bottom covers are installed.

2. Apply power to the counter and allow for a minumum warmup of 20 minutes. When possible a warmup of 24 hours is preferred.

3. Set counter controls and connections as defined in Section 4 of this manual ("Time Base Calibration").

4. Connect the 5 MHz (100 mV) frequency reference output to CHANNEL A input on the counter.

5. If necessary, adjust the time base so that the counter's display corresponds to the first reading presented in Table 6131-2. The adjustment is accessed through a hole in the left rear corner of the bottom case half. Use a JFD 5284 (or equivalent) non-ferrous adjustment tool. If installed at the rear of the bottom case half, the bail will have to be removed to allow access.

6. Change the counter's RESOLUTION setting to the next step listed in Table 6131-2 and repeat step (5) for the respective display. Display update in the 0.1 Hz setting occurs every ten seconds.

NOTE

When the OVFL LED is illuminated, observe the GATE LED (on) to verify that a measurement is being made.

6131-9. LIST OF REPLACEABLE PARTS

6131-10. A replacement oscillator can be ordered by using Fluke Part Number 484410. The Manufacturer's Federal Supply Code is 89536 and the Manufacturer's Part Number is 484410. The insulator can be ordered with part number 487710. Refer to Section 5 for ordering information.

Table 6131-2. Calibration

RESOLUTION	DISPLAY (±1 COUNT)
1 Hz	5000.000 kHz (7250A, 7260A, 7261A) 5.000000 MHz (7220A)
0.1 Hz	000.0000 kHz* (7250A) 5000.0000 kHz (7260A, 7261A) 5.0000000 MHz (7220A)

Option -132
Superior Low Power Oven Time Base

6132-1. INTRODUCTION

6132-2. The -132 Option is a crystal oscillator inside a temperature stabilized oven. The oven uses an extremely small amount of power. After the assembly is warmed up, power consumption is 1 watt, typically. This allows oven controlled time base accuracy with a battery powered instrument. Operation and Calibration of an instrument equipped with the -132 Option is the same as with a standard instrument. Refer to Sections 2 and 4 of this manual for additional information.

6132-3. SPECIFICATIONS

6132-4. The specifications of the -132 Option are listed in Table 6132-1.

6132-5. INSTALLATION

6132-6. Installation of the Superior Low Power Oven Time Base (Option -132) necessitates removal of the counter's Main PCB; refer to disassembly instructions included with Section 4. For each counter, the Superior Low Power Oven Time Base is installed in the top left rear corner of the Main PCB. Use the following installation procedure:

1. Unsolder and remove any other time base already installed.

2. Referring to Figure 6132-1, install the Superior Low Power Oven Time Base and insulator. Use the provided hardware to secure the time base to the Main PCB.

3. While exercising care not to overheat the multilayer Main PCB, solder the time base connections.

4. Complete jumper and solder bridge arrangements on the Main PCB as illustrated in Figure 6132-1 and described below:

a. 7220A: If necessary, remove the short at SB4 and jumper SB5 (bottom of Main PCB, left rear corner). Jumper SB2 (bottom, left front corner).

b. 7250A: If necessary, remove the short between W1 and +12V and jumper W1 to +5V (top of Main PCB, left front corner). Jumper SB2 (bottom of Main PCB, left front corner).

c. 7260A or 7261A: Remove the short at SB5 and jumper SB4 (bottom of Main PCB, left rear). Jumper SB2.

Table 6132-1. -132 Option Specifications

Nominal Frequency	10 MHz
Aging Rate	$\pm 3 \times 10^{-9}$/day*
	$\pm 5 \times 10^{-8}$/month*
Accuracy with Temperature (0° to 50°C)	$\pm 3 \times 10^{-8}$
Line Voltage (10% line variation)	$\pm 4 \times 10^{-9}$
Warmup	
10 minutes	$\pm 5 \times 10^{-7}$
20 minutes	$\pm 3 \times 10^{-8}$

* After 5 days continuous operation.

** Specifies offset from final frequency value (the value after 24 hours).

6132-7. CALIBRATION

6132-8. Calibration for the Superior Low Power Oven Time Base necessitates the use of a frequency reference

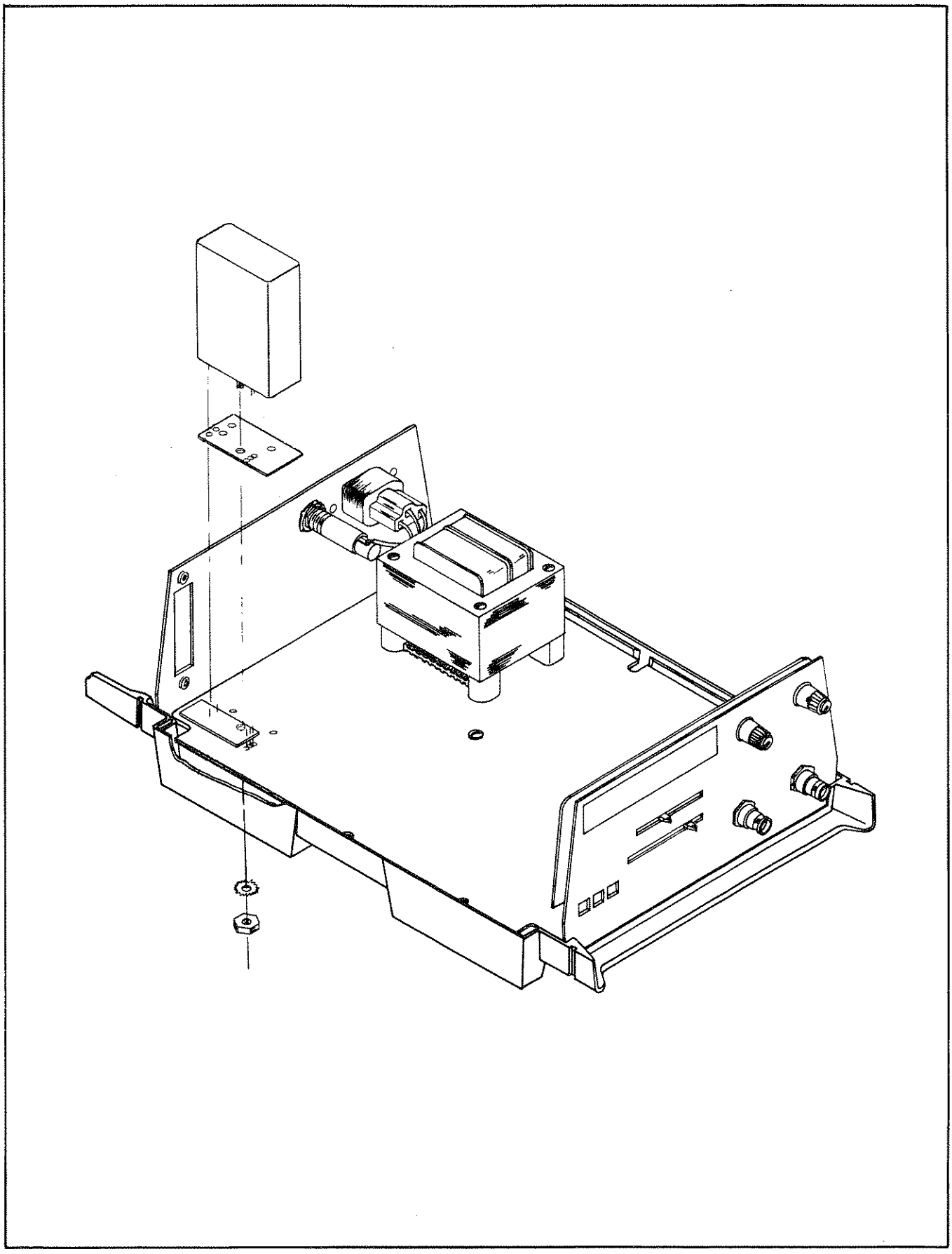


Figure 6132-1. Installation

with an accuracy of $\pm 1 \times 10^{9}$. A cesium standard, such as the HP 5061A, is recommended. This calibration procedure calls for applying the reference frequency to Channel A and adjusting the time base for a counter display of the known input. At the 0.1 Hz RESOLUTION setting on the counter, this method yields a demonstrated accuracy of 2 parts in 10^{8} (± 1 count error). Proceed with the following steps:

1. Ensure that the counter's top and bottom covers are installed.

2. Apply power to the counter and allow for a minumum warmup of 20 minutes. When possible a warmup of 24 hours is preferred.

3. Set counter controls and connections as defined in Section 4 of this manual ("Time Base Calibration").

4. Connect the 5 MHz (100 mV) frequency reference output to CHANNEL A input on the counter.

5. If necessary, adjust the time base so that the counter's display corresponds to the first reading presented in Table 6132-2. The adjustment is accessed through a hole in the left rear corner of the bottom case half. Use a JFD 5284 (or equivalent) non-ferrous adjustment tool. If installed at the rear of the bottom case half, the bail will have to be removed to allow access.

6. Change the counter's RESOLUTION setting to the next step listed in Table 6132-2 and repeat step (5) for the respective display. Display update in the 0.1 Hz setting occurs every ten seconds.

NOTE

When the OVFL LED is illuminated, observe the GATE LED (on) to verify that a measurement is being made.

6132-9. LIST OF REPLACEABLE PARTS

6132-10. A replacement oscillator can be ordered by using the Fluke Part Number 479121. The Manufacturer's Federal Supply Code is 89536 and the Manufacturer's Part Number is 479121.

Table 6132-2. Calibration

RESOLUTION	DISPLAY (±1 COUNT)
1 Hz	5000.000 kHz (7250A, 7260A, 7261A) 5.000000 MHz (7220A)
0.1 Hz	000.0000 kHz* (7250A) 5000.0000 kHz (7260A, 7261A) 5.0000000 MHz (7220A)

Option -521
Data Input/Output Unit

6521-1. INTRODUCTION

6521-2. The Data Input/Output Unit (Option -521) provides for remote control and sampling of instrument measurements. Measurement data can be exchanged when the I/O Unit is used in the 7220A or 7250A. When used in the 7260A or 7261A, the I/O Unit augments these features with full resolution, function and slope programming capabilities. A listing of signal lines referenced to each type of counter is presented in Table 6521-1. The I/O Unit is field installable using the procedures given under INSTALLATION. The unit may be ordered separately (use number 72XXA-521K).

6521-3. SPECIFICATIONS

6521-4. The -521 Option provides for serial BCD data transfer. Logic levels are TTL, low true. Speed is 60 readings per second.

6521-5. INSTALLATION

6521-6. The I/O Unit can be installed in the counter using the following procedure:

1. Press power to STBY and remove line power cord. Remove top and bottom case halves from the instrument. Refer to "Disassembly" in Section 4 for removal instructions. Remember that the case bottom is secured to the Main PCB Assembly with one central screw; prying the case top up while pressing down on the case bottom may damage the Main PCB.

2. On the instrument's rear panel, remove the "DATA OUT" dust cover.

3. Remove the screws securing the Rear Panel to the Main PCB Assembly.

   a. On the 7250A, remove the three screw securing the Rear Panel to the bottom of th Main PCB Assembly.

   b. On the 7220A, 7260A and 7261A, remov the six screws securing the heat sink to the rea panel.

4. Position the Rear Panel approximately 1/ inch back from the Main PCB.

5. Insert the I/O Unit, pcb first, through th "DATA" mounting port from the rear. (Refer t Figure 6521-1.)

6. Secure the I/O Unit rear connector to the Rea Panel with the supplied 4-40 mounting hardware

7. Route the flexible pcb around the instrument' time base and connect the I/O PCB connector to P on the instrument's Main PCB.

8. Install the screws securing the Main PCB to th Rear Panel.

9. Secure the Main PCB Assembly to the bottor case half.

10. Replace the top case half. Refer t Reassembly instructions provided in Section 4; cas halves must fit properly to ensure RFI shielding.

11. Using the instrument ribbon cable (Y7203 o Y7204) connect the Data I/O Unit to the desire interface (see Figure 6521-2).

Table 6521-1. Data Format Between Counter and I/O Unit (J4)

PIN NO.	FUNCTION	INSTRUMENT USED IN			
		7220A	7250A	7260A	7261A
1	Scan Oscillator Output from counter.	X	X	X	X
2	+5V	X	X	X	X
3	XB (Channel B Signal).		X	X	X
4	Measurement Unit	X	X	X	X
5	Decimal Point.	X	X	X	X
6	Remote Enable.	X	X	X	X
7	Main Gate from Counter	X	X	X	X
8	Busy signal from counter during measurement sequence.	X	X	X	X
9	Ground	X	X	X	X
10	Single continuous command to counter.	X	X	X	X
11	Start command to counter.	X	X	X	X
12	Function line F8 (to counter)			X	X
13	Function line F2			X	X
14	Function line F4			X	X
15	Function line F1			X	X
16	Resolution line R1 (to counter)			X	X
17	Resolution line R2			X	X
18	Resolution line R4			X	X
19	Bit 1 of BCD data from counter	X	X	X	X
20	Reset to counter		X	X	X
21	Positive slope command to Channel B			X	X
22	Positive slope command to Channel A			X	X
23	Filter command to counter			X	X
24	Digit Strobe Line 7 from counter	X	X	X	X
25	Digit Strobe 6	X	X	X	X
26	Digit Strobe 5	X	X	X	X
27	Digit Strobe 4	X	X	X	X
28	Digit Strobe 3	X	X	X	X
29	Digit Strobe 2	X	X	X	X
30	Overflow from counter	X	X	X	X
31	Digit Strobe 1	X	X	X	X
32	Bit 2 of BCD data from counter	X	X	X	X
33	Bit 4 of BCD data from counter	X	X	X	X
34	Bit 8 of BCD data from counter	X	X	X	X
35	Digit Strobe 8	X		X	X
36	Digit Strobe 9	X			

NOTE

Cable securing screws are supplied attached to the connectors on the Data I/O Unit and the Interface PCB Assembly.

6521-7. The I/O Unit can be removed from the instrument by following Installation steps 1 through 4 and the following:

1. Remove the two screws securing the I/O Unit connector to the Rear Panel.

2. Pry the I/O PCB connector away from the Main PCB (P4). Grasping the pcb at front and rear; gently work the unit free of P4. Avoid bending the Main PCB pins or excessively flexing the I/O PCB.

3. Withdraw the I/O Unit through the Rear Panel.

4. Complete "Installation" steps 8, 9 and 10.

6521-8. THEORY OF OPERATION

6521-9. The Data I/O Unit (Option -521) is illustrated on a functional block level in Figure 6521-3. Use this diagram in conjunction with the Schematic Diagram (located in Section 8) during the following circuit discussion.

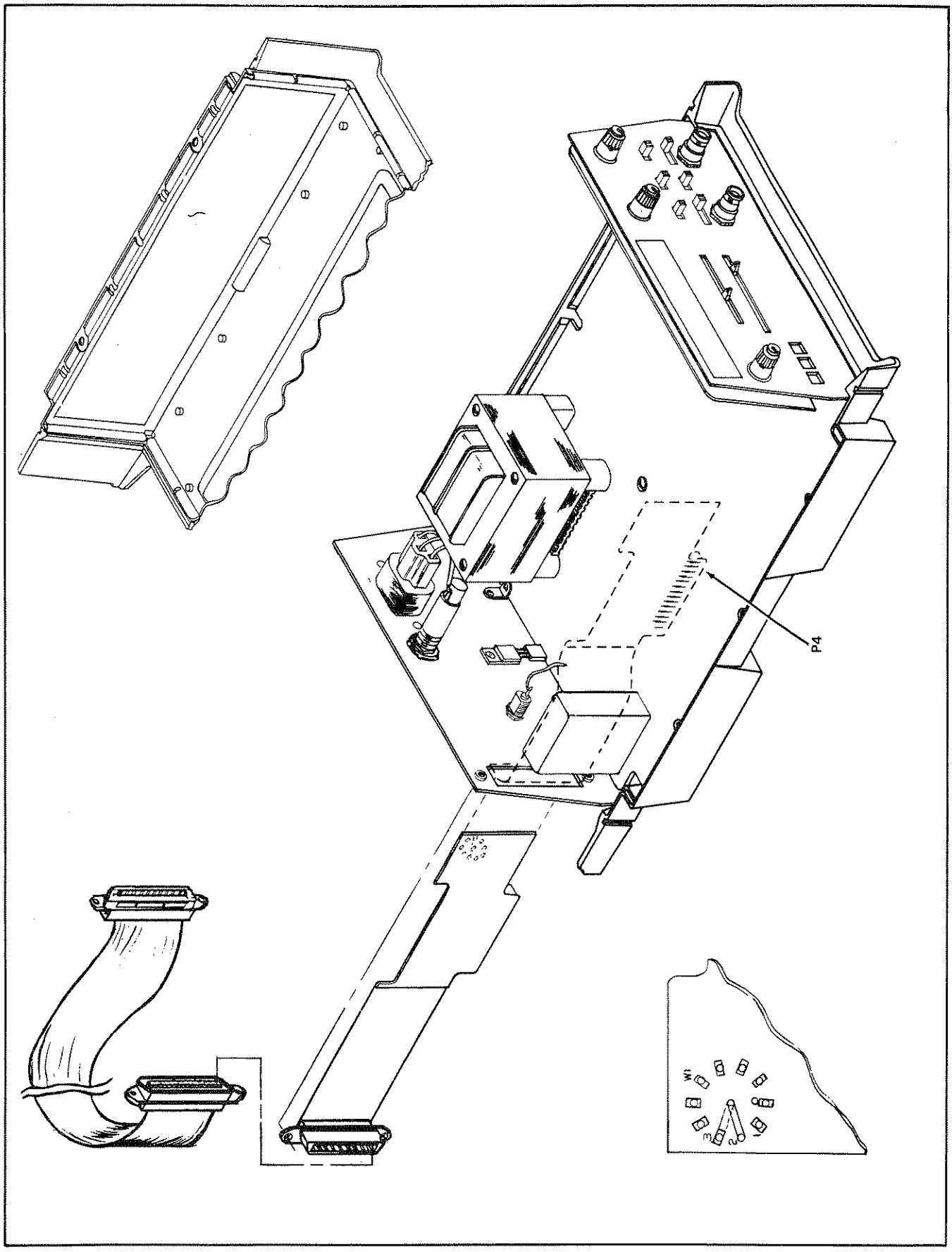


Figure 6521-1. Data Input/Output Unit Installation Details

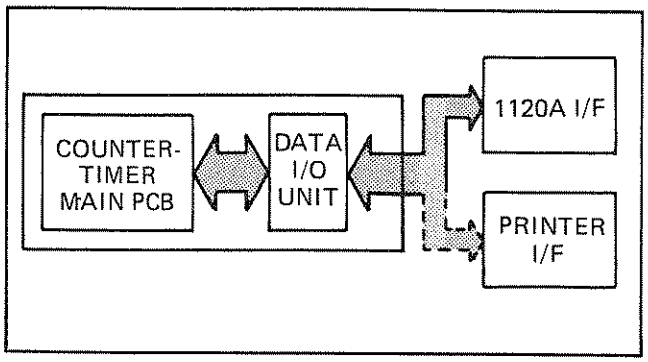


Figure 6521-2. Data I/O Unit Interconnections

6521-10. General

6521-11. The Data I/O Unit provides for buffered data transfers to and from the counter, and for address decoding when used with the 2020A or 2030A Printer Interface. The unit's circuitry operates in two basic modes, selectable by the state of the $\overline{\text{BUSEN}}$ line. When $\overline{\text{BUSEN}}$ is true, counter data is passed directly to the output. With $\overline{\text{BUSEN}}$ false, counter digit, decimal point and units data will not be output until the I/O Unit receives a valid address from an external device (such as the 2020A or 2030A).

6521-12. An address sent to the Data I/O Unit consists of a binary 4-bit code corresponding to decimal numbers 1 through 10. An address select jumper can be positioned on the Data I/O PCB for the desired valid address. When the received address matches the jumpered address, the Data I/O PCB will respond with an $\overline{\text{ADRVAL}}$ signal (true).

6521-13. After gathering the next reading, the counter will output $\overline{\text{DATVAL}}$ true pulses at the center of each digit strobe time. This sequence is illustrated in Figure 6521-4. Note that $\overline{\text{DATVAL}}$ pulses begin with DS1, and continue from most significant to least significant digit. Only one sequence of $\overline{\text{DATVAL}}$ pulses will occur for each measurement cycle. If $\overline{\text{ADRVAL}}$ is removed in the middle of an output sequence, $\overline{\text{DATVAL}}$ will be asserted not true. If $\overline{\text{ADRVAL}}$ is then asserted true again, a new measurement cycle must be completed before data is output.

6521-14. With the $\overline{\text{REM}}$ line true, the counter's measurement cycle can be controlled by an external device. Each new measurement cycle will now begin after the START signal is pulsed true.

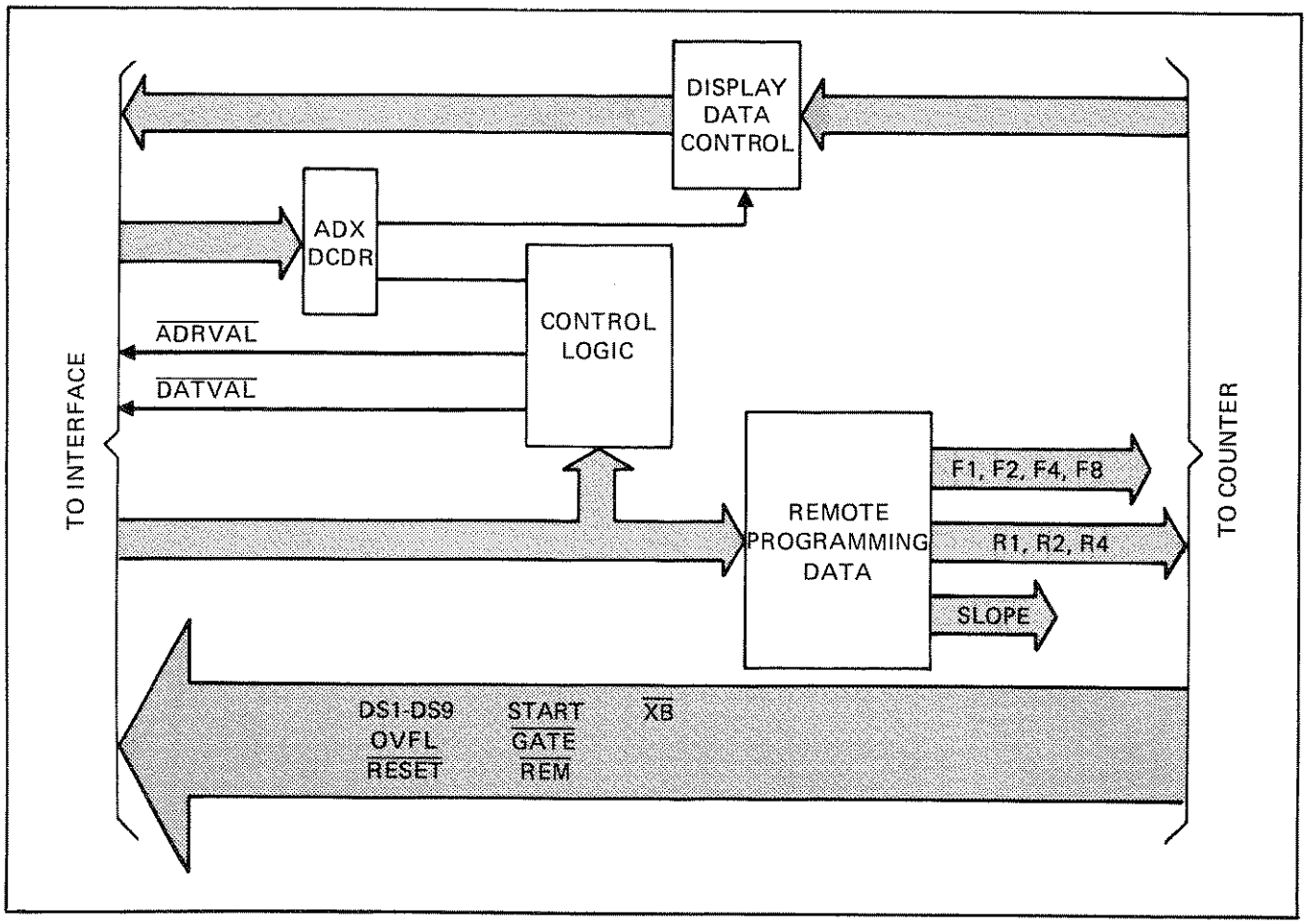


Figure 6521-3. Block Diagram, Input/Output Unit (Option -521)

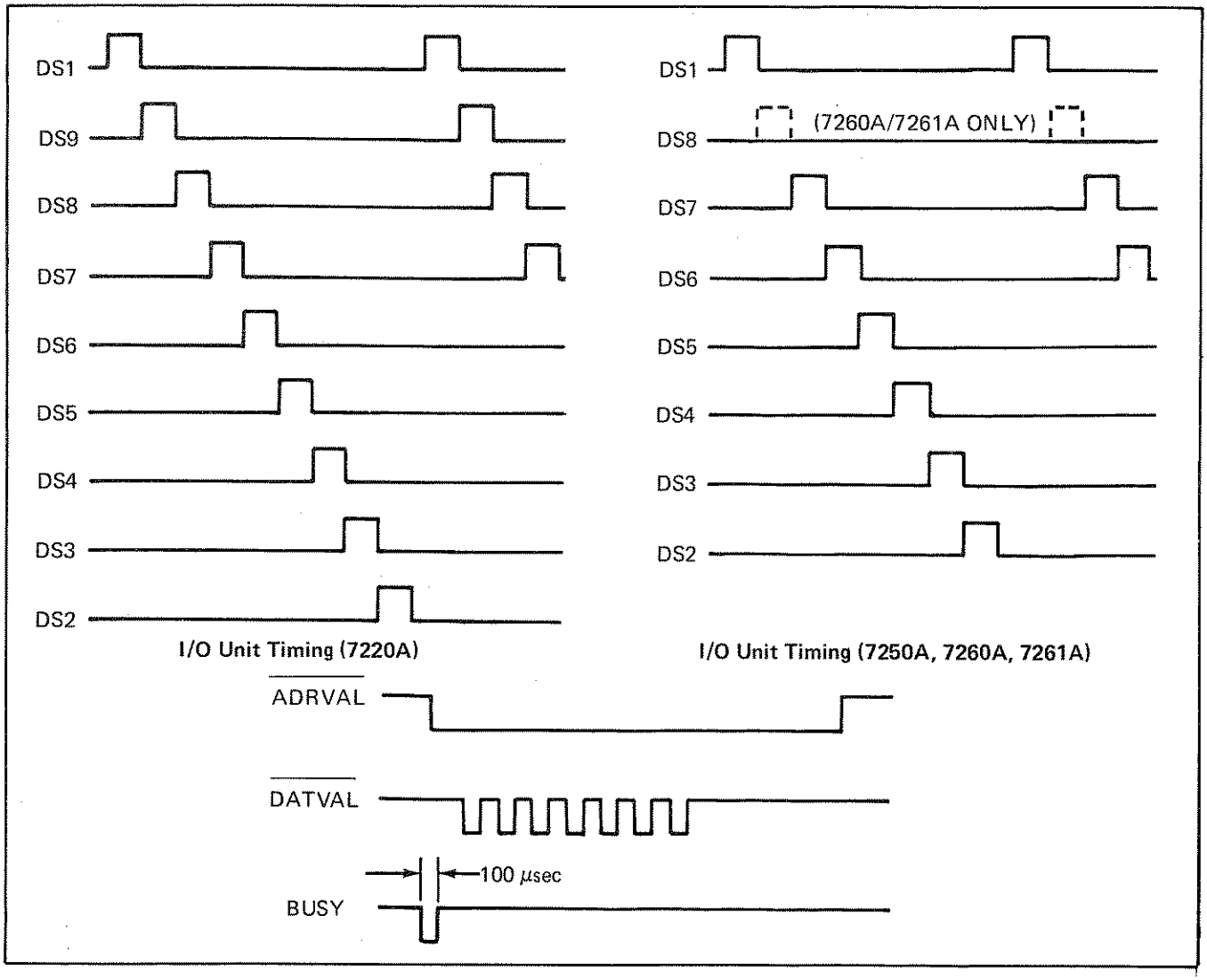


Figure 6521-4. I/O Unit Timing

6521-15. Data Management Logic

6521-16. The I/O Unit provides 36 data lines to the instrument at J4. Lines in use will vary for each instrument; refer to Table 6521-1 for a description of data lines by function and relevant instrument. Many data lines, e.g., digit strobe lines, are simply routed through the I/O Unit without control. Display data lines from the instrument are routed through tri-state buffers in U1. When used, the 1120A will hold $\overline{\text{BUSEN}}$ low to enable these buffers through U3-4. With the 2020A or 2030A, $\overline{\text{BUSEN}}$ is held high and a properly decoded address places a high at U3-13, again enabling the buffers through U3-4. Remote programming data to the instrument (function, resolution and slope) is routed through tri-state buffers controlled by the $\overline{\text{REM}}$ line.

6521-17. Printer Control Logic

6521-18. The following circuit description is valid when the Data I/O Unit is used with a Printer Interface (2020A or 2030A). The printer interface uses pins 1 through 18 on the interface connector J5. To strobe display digit data to the interface, the instrument's scan oscillator is sampled to derive a data valid ($\overline{\text{DATVAL}}$) reference pulse. These pulses are routed through U3-10 and U4-11 when the following conditions are met. First, a valid address from the printer interface must be decoded to enable U4-11. Secondly, D flip-flop U2-13 must go high to enable NAND gate U3-10. The negative going edge of the internal START pulse will now trigger the instrument. After the measurement sequence is completed, a not busy (BY) signal is returned to clock D flip-flop U2-1 high. The next digit strobe from the instrument on DS1 will now clock D flip-flop U2-13 high, enabling the $\overline{\text{DATVAL}}$ pulses. A DATVAL pulse will now accompany each digit of parallel display information (B1, B2, B4, B8, DP, UX). The high on U2-13 also resets D flip-flop U2-1, placing a low at the D input to flip-flop U2-13. The next DS1 strobe will clock U2-13 low and disable $\overline{\text{DATVAL}}$ pulses. Digit strobe lines DS1-DS9 are not otherwise used with the printer interface. All digits are thereby strobed once for

each START pulse sent to the instrument and each not BY signal returned to the I/O Unit.

6521-19. Address Decode Logic

6521-20. When used with a printer interface (2020A or 2030A), the I/O Unit must be separately addressed. Valid addresses, using lines F2, F8, F1 and HOLD, are decoded by U5 and the jumpering arrangement of W1. For the 7250A, 7260A and 7261A, address 2 is valid; address 3 is used for the 7220A. A decoded address serves three functions: display data buffers are enabled, printer control buffers U4-11 and U4-13 are enabled, reset is released on D flip-flop U2-13 and the D input at U2-5 is set.

6521-21. DATA FORMAT

6521-22. Data lines used between the counter and the Data I/O Unit will vary with the type of counter in use. Table 6521-1 defines J4 lines in use for each counter.

6521-23. The data format used between the Data I/O Unit and the interface will vary with the type of interface in use. Of the lines available at P5, the 1120A IEEE-488 interface will use all 36 and the 2020A or 2030A interface will use only the first 18. Table 6521-2 defines line usage for both types of interface.

6521-24. PERFORMANCE TEST

6521-25. A performance test for the Data I/O Unit is included with the overall IEEE Interface System check-out and troubleshooting procedure in Option -529.

6521-26. TROUBLESHOOTING

6521-27. Troubleshooting procedures are included in Option -529 information.

6521-28. REPLACEABLE PARTS

6521-29. A detailed list of replaceable parts is presented in Table 6521-3. Figure 6521-5 can be used as an aid in locating components. Refer to Section 5 for parts ordering information.

Table 6521-2. Data Format Between Interface and I/O Unit

PIN NO.	1120A MNEMONIC	1120A FUNCTIONAL DESCRIPTION	2020A/2030A MNEMONIC	2020A/2030A FUNCTIONAL DESCRIPTION
1	B+	Positive slope command to Channel B.	ADRVAL	Address Valid indicates to printer that instrument with this address is present and is responding.
2	A+	Positive slope command to Channel A.	DATVAL	Data Valid is sent from the instrument to synchronize data.
3	F2	Function command line to instrument.	A0	Address line used by printer to select an instrument.
4	F8	Function command line to instrument.	A1	Address line.
5	F1	Function command line to instrument.	A2	Address line.
6	HOLD		A3	Address line.
7	F4	Function command line to instrument.	ACK	Acknowledge signal.
8	FILTER	Filter command to instrument.	SCAN	Sent by instrument to indicate a scanner is present.
9	D1	BCD digit (1)	D0	BCD digit (1) data or ASCII bits (lwr).
10	D2	BCD digit (2)	D1	BCD digit (2) or Lower ASCII.
11	D3	BCD digit (4)	D2	BCD digit (4) or Lower ASCII.
12	D4	BCD digit (8)	D3	BCD digit (8) or Lower ASCII.
13	DP	Decimal point command	D4	Decimal point with BCD or Upper ASCII.
14	UX	Measurement unit command	D5	Measurement unit with BCD or Upper ASCII.
15	R4	Resolution command to counter.	D6	Upper ASCII.
16	R2	Resolution command	D7	Upper ASCII.
17	GND	Ground	GND	Ground
18	R1	Resolution command	+5	+5V supplied by printer for isolated DOU.
19	REM	Remote command to counter.		Not used.
20	S6	Digit Strobe 6 from counter.		Not used.
21	S5	Digit Strobe 5.		Not used.
22	BUSEN	Data buffer enable		Not used.
23	XB	Channel B signal		Not used.
24	GATE	Main Gate enable signal from counter.		Not used.
25	START	Measurement sequence start command to counter.		Not used.
26		Not used.		Not used.
27	BUSY	Measurement sequence in progress from counter.		Not used.
28	S8	Digit Strobe 8		Not used.
29	S9	Digit Strobe 9.		Not used.
30	S7	Digit Strobe 7		Not used.
31	S2	Digit Strobe 2		Not used.
32	S3	Digit Strobe 3		Not used.
33	OVRFLW	Overflow from counter		Not used.
34	S4	Digit Strobe 4		Not used.
35	RESET	Reset command to counter		Not used
36	S9	Digit Strobe 9 (from 7220A)		Not used.

Table 6521-3. Data Input/Output PCB Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	⊘ DATA INPUT/OUTPUT PCB ASSEMBLY FIGURE 6521-5 OPTION -521 (7220A-4007T)	487454	89536	487454	1		
CR1	DIODE, SI, HI-SPEED SWITCH	203323	07910	1N4448	1	1	
J4	CONNECTOR, 36-PIN	484733	00779	87406-1	1		
MP1	INTERFACE, PCB	487439	89536	487439	1		
P5	CONNECTOR, 36-PIN	479493	00779	552817-1	1		
R1	RES, DEP. CAR, 100K +/-5%, 1/4W	348920	80031	CR251-4-5P100K	1		
RN1	RES, NETWORK, 33K	484741	89536	484741	1	1	
U1	⊘ IC, C-MOS, HEX NON INVET BUFFERS	407759	04713	MC14503CP	1	1	
U2	⊘ IC, C-MOS, DUAL TYPE "D" FLIP-FLOP	340117	04713	MC14013CP	1	1	
U3	⊘ IC, C-MOS, QUAD, 2-INPUT NAND GATES	355198	04713	MC14011CP	1	1	
U4	IC, TRI-STATE HEX BUFFER	483800	89536	483800	1	1	
U5	⊘ IC, C-MOS, BCD TO DECIMAL DECODER	380741	01295	TP4028AN	1	1	
U6	IC, LO-PWR, SCHOTTKY TRI-ST OCTAL, BFR.	429902	12040	DM81LS95N	1	1	
W1	PLUG, JUMPER	416895	91506	8136-650P2	1		
W1.	--SOCKETS	376418	89536	376418	15		

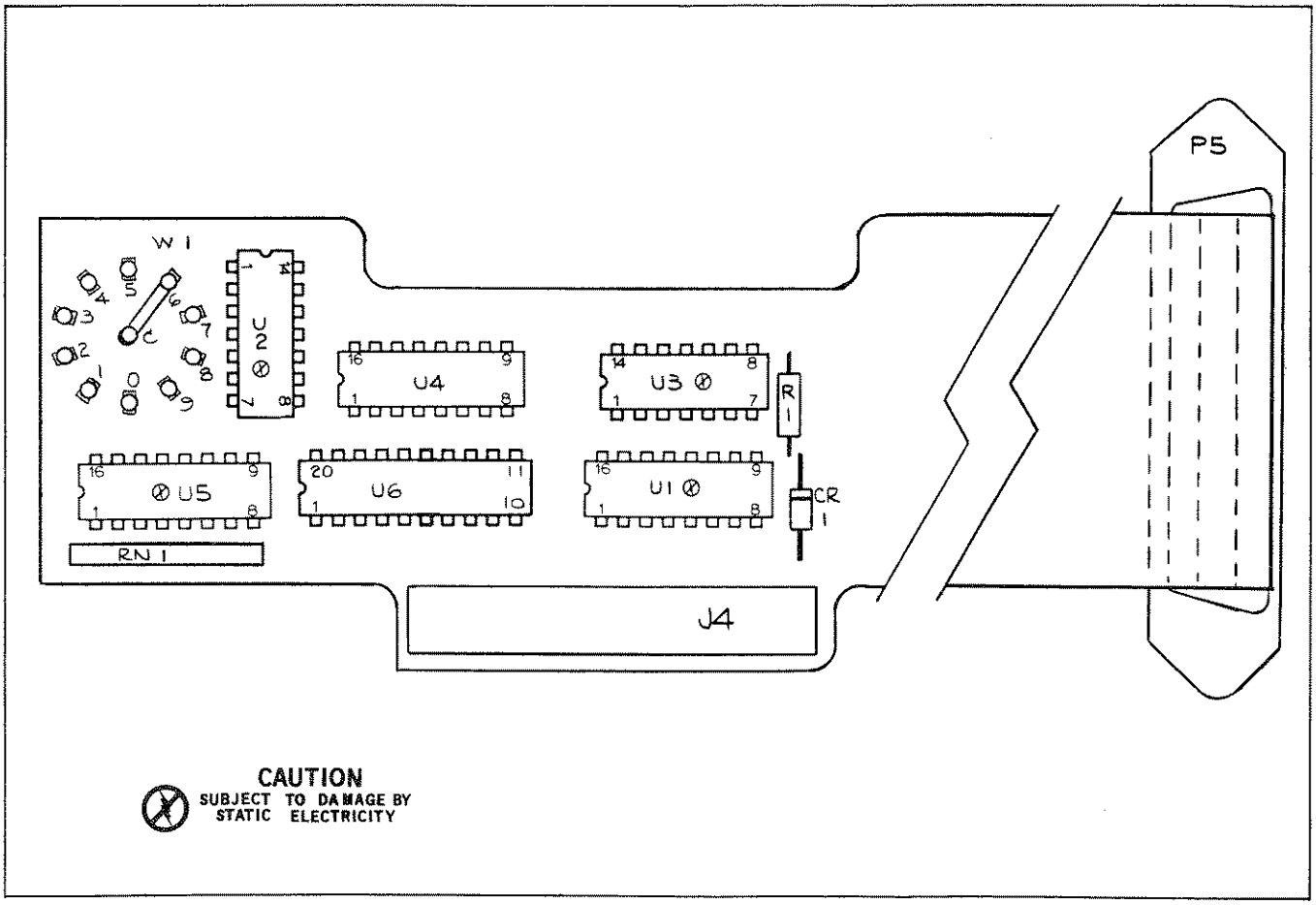


Figure 6521-5. Data Input/Output PCB Assembly

Option -522
Interface PCB Assembly

6522-1. INTRODUCTION

6522-2. The Interface PCB Assembly provides for data interchange between the IEEE-488 bus and the counter. The unit is field installable using procedures given under INSTALLATION. It may be ordered separately (72XXA-522K) or as part of the IEEE Interface Option (72XXA-529K).

6522-3. INSTALLATION

6522-4. The Interface PCB Assembly is installed in and supported by the 1120A IEEE-488 Translator. The following steps provide a method for installing and connecting the Interface in an IEEE bus system. Interconnections are illustrated in Figure 6522-1.

1. On the 1120A, place the power switch to STBY and remove the line power cord.

2. On the 1120A case bottom, remove the four case securing screws. Lift the case top clear of the 1120A.

3. Locate the Interface PCB Assembly positions on the Main PCB (left side). Refer to Figure 6522-2. These positions are labeled IF0, IF1 and IF2 on the Main PCB, corresponding respectively to device 0, 1 and 2 as identified on the instrument's front panel.

4. Grasp the Interface PCB Assembly at both upper corners.

NOTE

Avoid touching circuitry on the Interface PCB Assembly.

5. Install the Interface PCB Assembly in the desired interface position. Ensure that the Assembly fits in the front panel guide slot, and that the grooved connector on the rear of the pcb fits into the rear panel guide.

6. Applying equal pressure at front and rear, press the Assembly into its jack on the Main PCB.

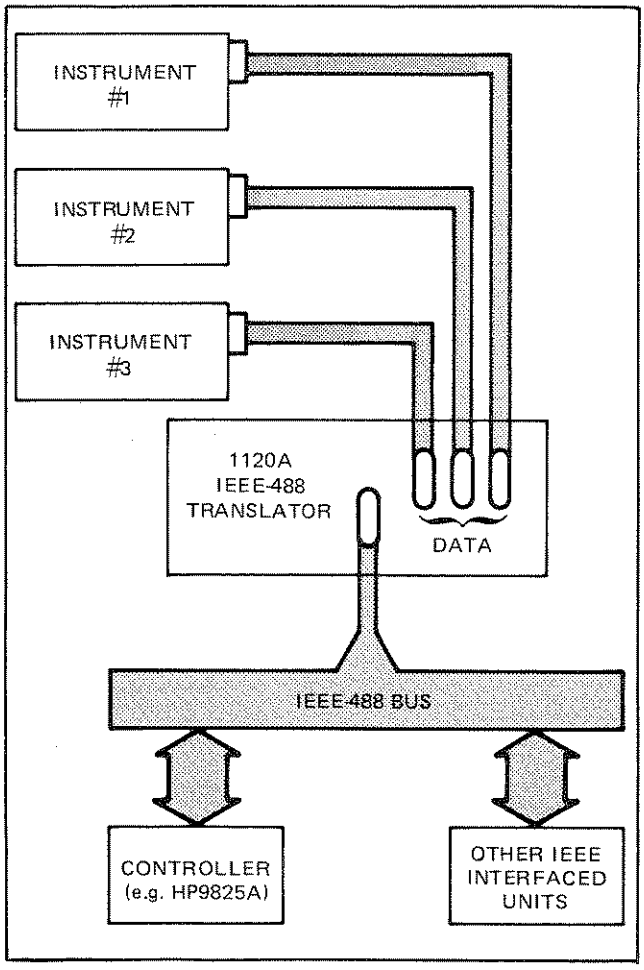


Figure 6522-1. Interface System Conections

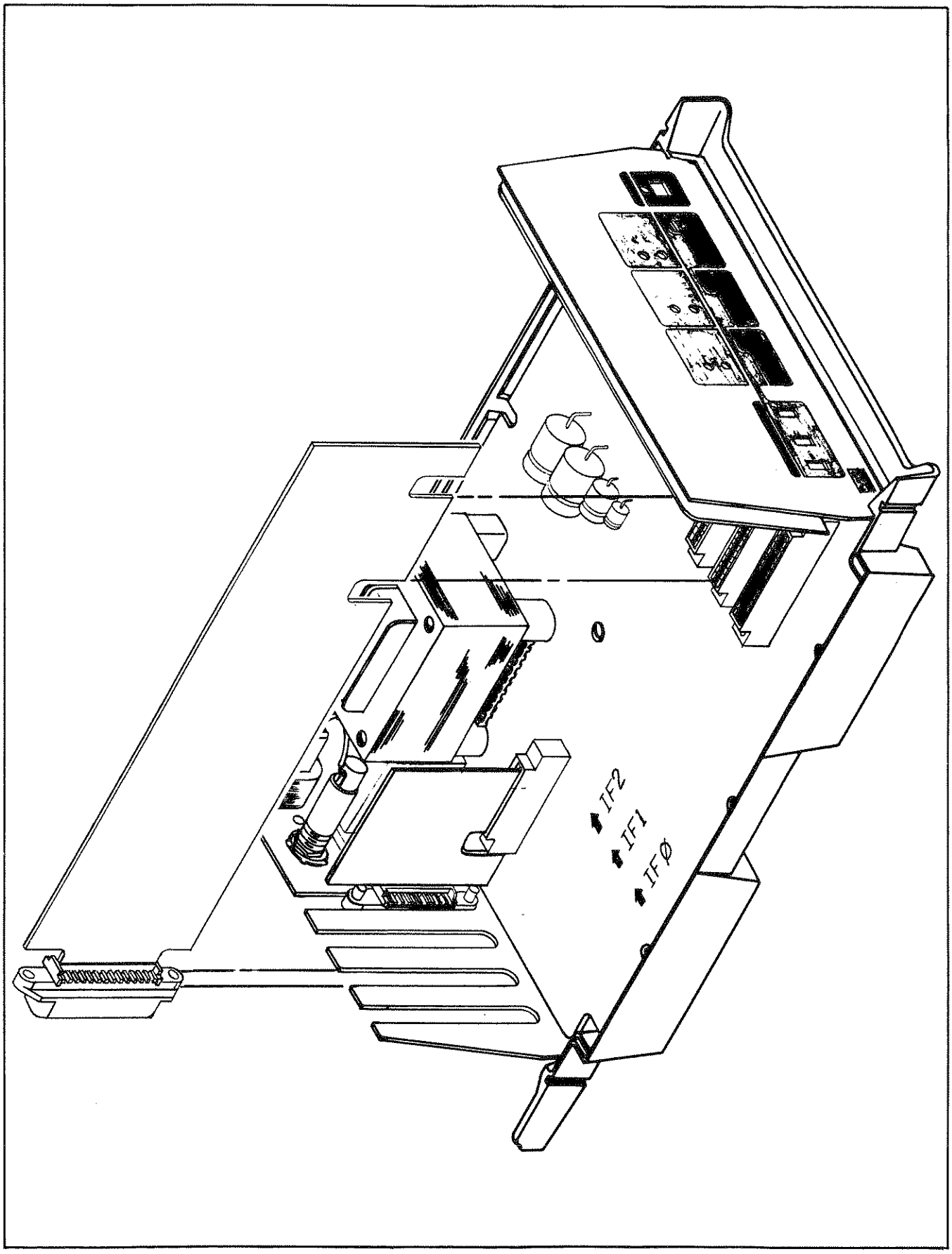


Figure 6522-2. Interface PCB Installation

7. Replace the 1120A's top cover.

8. Connect the 1120A to a bus controller using a standard IEEE bus cable (Fluke accessory numbers, Y8001, Y8002 or Y8003).

9. Connect the Interface PCB Assembly to the measurement instrument's Data I/O Unit using a standard instrument cable (Fluke accessory numbers Y7203 or Y7204). Cable securing screws are supplied attached to the Interface PCB Assembly connector.

10. Energize the 1120A.

6522-5. THEORY OF OPERATION

6522-6. Functional Description

6522-7. The Interface PCB Assembly, when addressed as a listener or talker on the bus, translates IEEE-488 codes and signals for compatible communications with measurement instruments. When addressed as a listener, each plug-in interface assembly will receive programming codes from a controller; when addressed to talk, the pcb will send data from the measurement instrument. Figure 6522-3 provides a functional block outline of Interface operation.

6522-8. The Interface System Processor function provides routing and control of measurement instrument data via the internal data bus. This processor will receive programming data from the IEEE Processor function and control the measurement instrument data gathering process through the Output functional block. The System Processor will also communicate measurement instrument data from the Input functional block to the IEEE processor.

6522-9. The IEEE Processor handles handshake and bus management operations for the external IEEE bus. This function will also signal the Interface System Processor, via an interrupt, of measurement instrument data being transferred to and from the external IEEE bus. Each Interface PCB Assembly installed in the 1120A is assigned a distinct address. The IEEE bus controller then addresses and, and using this address, handshakes with the Interface PCB Assembly.

6522-10. Interface Operation Cycle

6522-11. The following discussion is referenced to the flow diagram in Figure 6522-4. Mnemonics used in the diagram and in this discussion are defined in Table 6522-1. The operation cycle consists of six states (S1-S6). Interchanges between the IEEE-488 bus and the Interface can occur only during S1, S4 or S6. The time during each

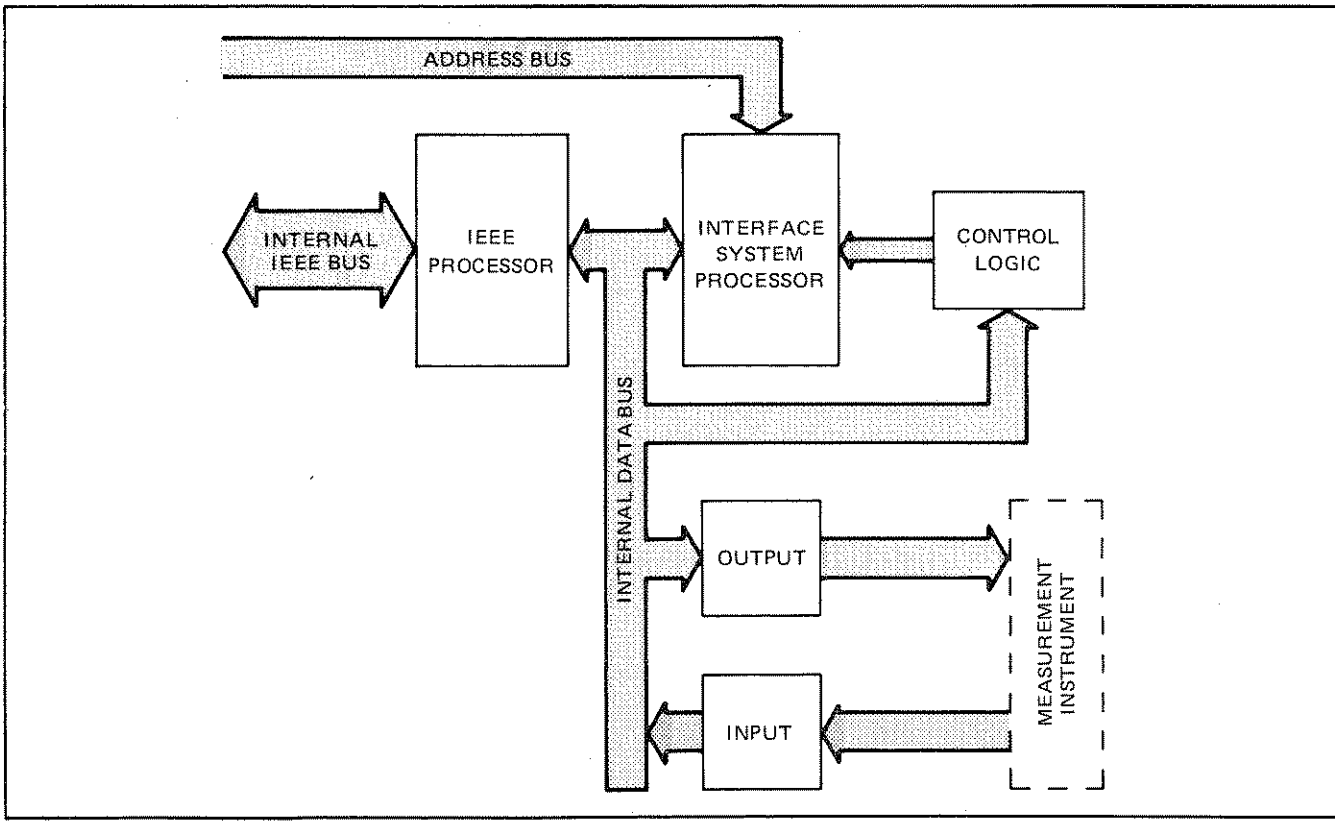


Figure 6522-3. Interface Functional Block Diagram

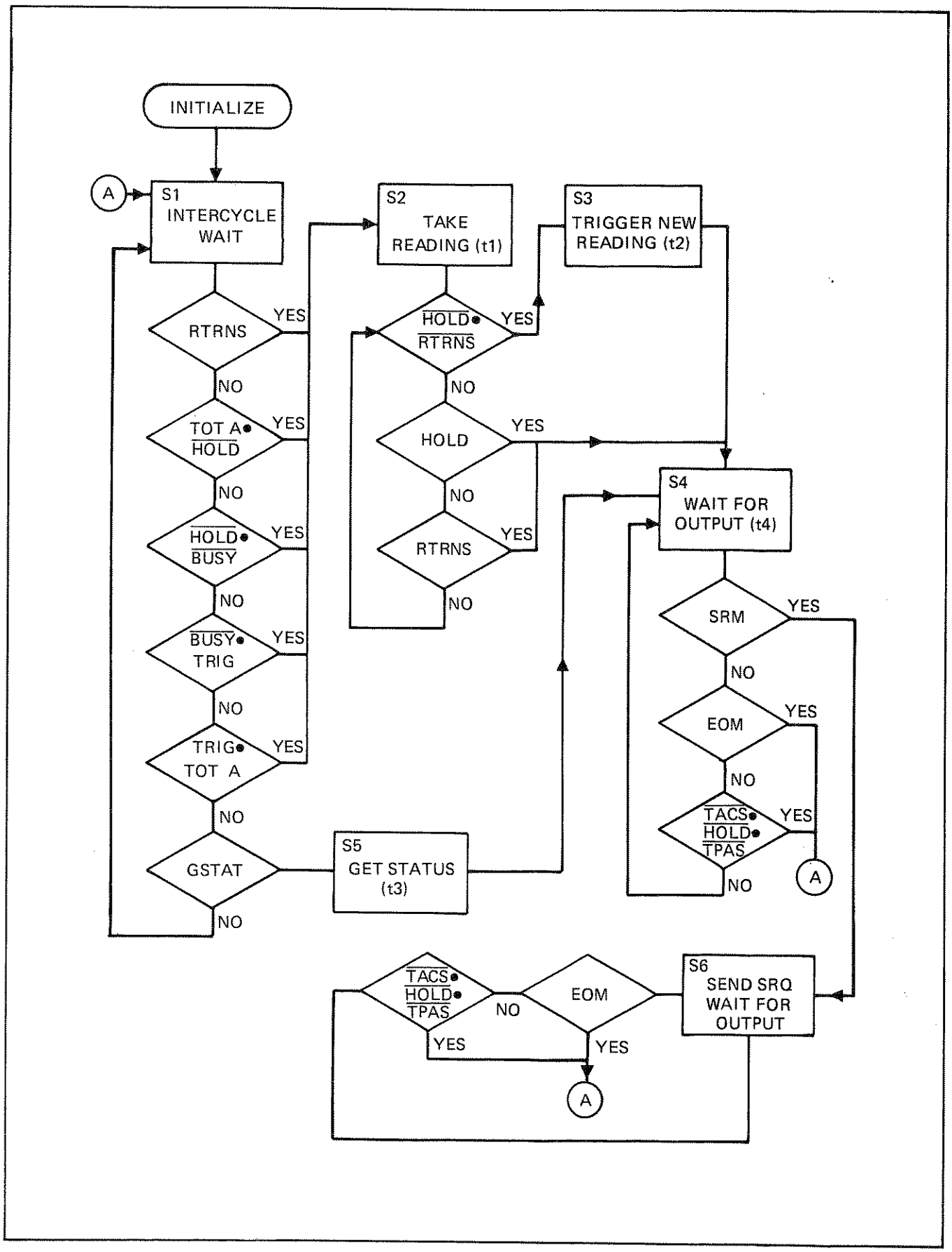


Figure 6522-4. Interface Operation Cycle

of these three states can be divided into the following two variable segments:

1. Interface Message Active (IMAS), during which messages from the IEEE bus (e.g., programming commands) are received and buffered. Instrument readings (data gathered during S2) can be output to the bus.

2. Remote Progam Active (RPAS), during which device messages stored in the receive buffer are executed. Once this segment is begun, all stored messages must be executed before the state is terminated. Allowable remote programming messages are listed in Table 6522-2.

6522-12. During the Intercycle Wait State (S1), the interface waits for commands from either the IEEE bus or the instrument. If GSTAT becomes true, the interface will proceed to the Get Status State (S5). Otherwise, the interface will proceed with a reading (S2) when the required conditions are met.

6522-13. The Take Reading State (S2), proceeds for a period termed t1. During this time, the interface will receive, format and place into an internal buffer all display digit data, measurement units and decimal point data. Once this process is complete, the interface will proceed to the Trigger New Reading State (S3), if the HOLD and RTRNS conditions are false. If either condition is true, the Interface will proceed directly to Wait for Output State (S4). During Trigger New Reading (S3), the interface will output a trigger (START) to the instrument.

6522-14. The Interface will require a time t2 to generate a trigger signal. It will then proceed to S4 (Wait for Output), during time t2. In S4, the interface is either waiting to output or is outputting a reading from its internal buffer to the bus. If in the service request mode (SRM), the interface will now traverse from S4 to S6. Otherwise, a transition will be made back to S1 when the required conditions are met. When in the service request mode (S6), the interface will output the SRQ message to the bus and then proceed back to S1 when the output is completed.

6522-15. PROGRAMMING COMMANDS

6522-16. The Interface PCB Assembly provides for bidirectional data transfer between the IEEE-488 bus and a measurement instrument. Programming commands from the IEEE bus are defined by function and applicable instrument in Table 6522-2. Code applicability will vary among instruments. For example, Resolution and Function programming can be used with the 7260A and the 7261A, but not with the 7220A or the 7250A.

Table 6522-1. Mnemonics (for Interface Operation Cycle)

MNEMONIC	DESCRIPTION
BUSY	Busy is sent true when instrument measurement sequence is in progress.
EOM	End of Message (indicates output complete).
GSTAT	Get Status state, set true by "G" command code.
HOLD	Hold mode. "H1" command code sets this state true.
RTRNS	Retransmit. This state is set true when the "X" command code is received.
SRM	Service Request Mode (Set by "M1" command code).
SRQ	Service Request (IEEE interface signal).
TACS	Interface Active as a Talker.
TOT A	Totalize Channel A. The instrument will output BY continuously when set to Totalize mode (7250A). This mode is termed "A X B" in the 7260A or 7261A. The F9 code must then be sent to enable totalize readings (proceed to S2).
TPAS	Interface Addressed as a Talker.
TRIG	Trigger state set true by "T" command code.
t1	Time required for interface to gather and format instrument data.
t2	Time required to generate a trigger pulse.
t3	Time required to gather instrument status.
t4	Minimum time required to output buffered reading.

Table 6522-2. Programming Commands

CODE	DESCRIPTION		USED WITH			
			7220A	7250A	7260A	7261A
F0	FREQ A	FUNCTION COMMANDS			X	X
F1	Ratio A/B				X	X
F2	Period A				X	X
F3	Period Average A				X	X
F4	Time Interval				X	X
F5	Time Interval Average				X	X
F6	Frequency C				X	X
F7	Self Check				X	X
F8	Counts Per Minute				X	X
F9	Totalize (with the 7250A, F9 must be sent for remote operations if instrument has been manually set to TOT A)			X	X	X
R0	10^0/100 μs	RESOLUTION COMMANDS			X	X
R1	10^1/1 ms				X	X
R2	10^2/10 ms				X	X
R3	10^3/100 ms				X	X
R4	10^4/1s				X	X
R5	10^5/10s				X	X
R7	AUTO				X	X
C	Clears previous operating modes to the preset condition (M0, H0, J0)		X	X		
	Clears to (M0, H0, J0, F0, R0, A+, B+, D0)				X	X
E	Reset instrument (display will clear and instrument begins a new reading if not in HOLD).			X	X	X
G	Get Status. For each "G" command, status is gathered once from the instrument and placed in an output buffer. Status is output the next time a reading is requested over the bus.		X	X	X	X
H0	Continuous trigger mode in which the instrument automatically cycles through the measurement routine.		X	X	X	X
H1	Hold mode, in which a new reading is initiated by the instrument only after a trigger command is received via the IEEE-488 interface.		X	X	X	X
J0	No line feed suppression on output.		X	X	X	X
J1	Line feed suppression on output.		X	X	X	X
M0	No Service Request.		X	X	X	X
M1	SRQ is sent after the instrument reading has been gathered.		X	X	X	X
T	Trigger. Sets Interface Trigger state and End of Message state true.		X	X	X	X
X	Retransmit. Sets RTRNS state in Interface true.		X	X	X	X

Table 6522-2. Programming Commands (cont)

CODE	DESCRIPTION	USED WITH			
		7220A	7250A	7260A	7261A
A+	Set slope for Channel A.			X	X
A–				X	X
B+	Set slope for Channel B.			X	X
B–				X	X
D0	Disengage 100 kHz filter.			X	X
D1	Engage 100 kHz filter.			X	X

6522-17. PERFORMANCE TEST

6522-18. Performance testing for the Interface PCB Assembly is included with overall IEEE system test presented with Option -529.

6522-19. TROUBLESHOOTING

6522-20. Troubleshooting procedures are covered in the Option -529 system tests.

6522-21. REPLACEABLE PARTS

6522-22. Table 6522-3 provides a detailed parts breakdown of the Interface PCB Assembly. Figure 6522-5 offers an aid in component location. Refer to Section 5 for parts ordering information.

Table 6522-3. Interface PCB Assembly

ITEM NO.	DESCRIPTION	FLUKE STOCK NO.	MFG SPLY CODE	MFG PART NO. OR TYPE	TOT QTY	REC QTY	USE CDE
	Ⓐ INTERFACE P.C.B. OPTION-522 FIGURE 6522-5 (1120A-4004T)	476465	89536	476465			
C1	CAP, MICA, 22 PF +/-5%, 500V	148551	72136	DM15220	2		
C2	CAP, TA, 1 UF +/-20%, 35V	161919	56289	196D010X0035G	1		
C3	CAP, CER, 0.1 UF, GMV, 10V	368647	71590	UK10-104	2		
C4	CAP, CER, 0.1 UF, GMV, 10V	368647	71590	UK10-104	REF		
C5	CAP, CER, 10,000 PF +/-20%, 100V	149153	56289	C023B101F103M	4		
C6	CAP, CER, 10,000 PF +/-20%, 100V	149153	56289	C023B101F103M	REF		
C7	CAP, CER, 10,000 PF +/-20%, 100V	149153	56289	C023B101F103M	REF		
C8	CAP, CER, 10,000 PF +/-20%, 100V	149153	56289	C023B101F103M	REF		
C9	CAP, MICA, 22 PF +/-5%, 500V	148551	72136	DM15220	REF		
CR1	DIODE, SI	343491	04713	1N4002	1	1	
H1	HARDWARE KIT	484196	00779	552568-1	1		
H2	WASHER	110775	89536	110775	2		
J1	CONNECTOR, 36-PIN	484170	00779	552238-1	1		
L1	CHOKE, RF	147835	72259	WEE220	1		
R2	RES, COMP, 4.7K +/-5%, 1/4W	348821	01121	CB4725	1		
R3	RES, COMP, 100K +/-5%, 1/4W	348920	01121	CB1045	2		
R4	RES, COMP, 4.7K +/-5%, 1/4W	348821	01121	CB4725	REF		
R5	RES, COMP, 100K +/-5%, 1/4W	348920	01121	CB1045	REF		
R6	RES, COMP, 510 +/-5%, 1/4W	441600	01121	005115	1		
RN1	RES NET, 100K +/-2%, 1/8W	461038	89536	461038	3		
RN2	RES NET, 100K +/-2%, 1/8W	461038	89536	461038	REF		
RN3	RES NET, 4.7K +/-2%, 1/8W	412916	89536	412916	1		
RN4	RES NET, 4.7K +/-2%, 1/8W	484063	89536	484063	1		
RN5	RES NET, 100K +/-2%, 1/8W	461038	89536	461038	REF		
RN6	RES NET, 100K +/-2%, 1/8W	412726	89536	412726	1		
S1	SWITCH, SLIDE, SPDT, 125V	453365	79727	G1-116-0001 G20-52	1		
U1	IC, DIGITAL	477794	04713	MC68488P	1	1	
U2	IC, N-CHAN	473066	34649	8048C	1	1	
U3	Ⓐ TC, C-MOS, HEX, NON-INVERT BUFFER	407759	12040	MM80C97N	3	1	
U4	Ⓐ TC, C-MOS, HEX, NON-INVERT BUFFER	407759	12040	MM80C97N	REF		
U5	IC, TTL, POS/NAND, HEX INVERTER	394536	01295	SN74LS05	1	1	
U6	Ⓐ TC, C-MOS, QUAD CLOCK, D-LATCH	355149	02735	CD4042AE	1	1	
U7	IC, LINE DECODER	408716	01295	SN74LS42N	1		
U8	IC, TTL, FLIP/FLOP	473223	01295	SN74LS374	2	1	
U9	TC, TTL, MSI	408377	01295	SN74LS75N	1	1	
U10	IC, TTL, MSI	393033	01295	SN74LS00	1	1	
U11	Ⓐ IC, C-MOS, HEX NON-INVERT BUFFER	407759	12040	MM80C97N	REF		
U12	IC, TTL, FLIP/FLOP	473223	01295	SN74LS374	REF		
XU1	SOCKET, IC, 40-PIN	429282	09922	DILB40P-108	2		
XU2	SOCKET, IC, 40-PIN	429282	09922	DILB40P-108	REF		

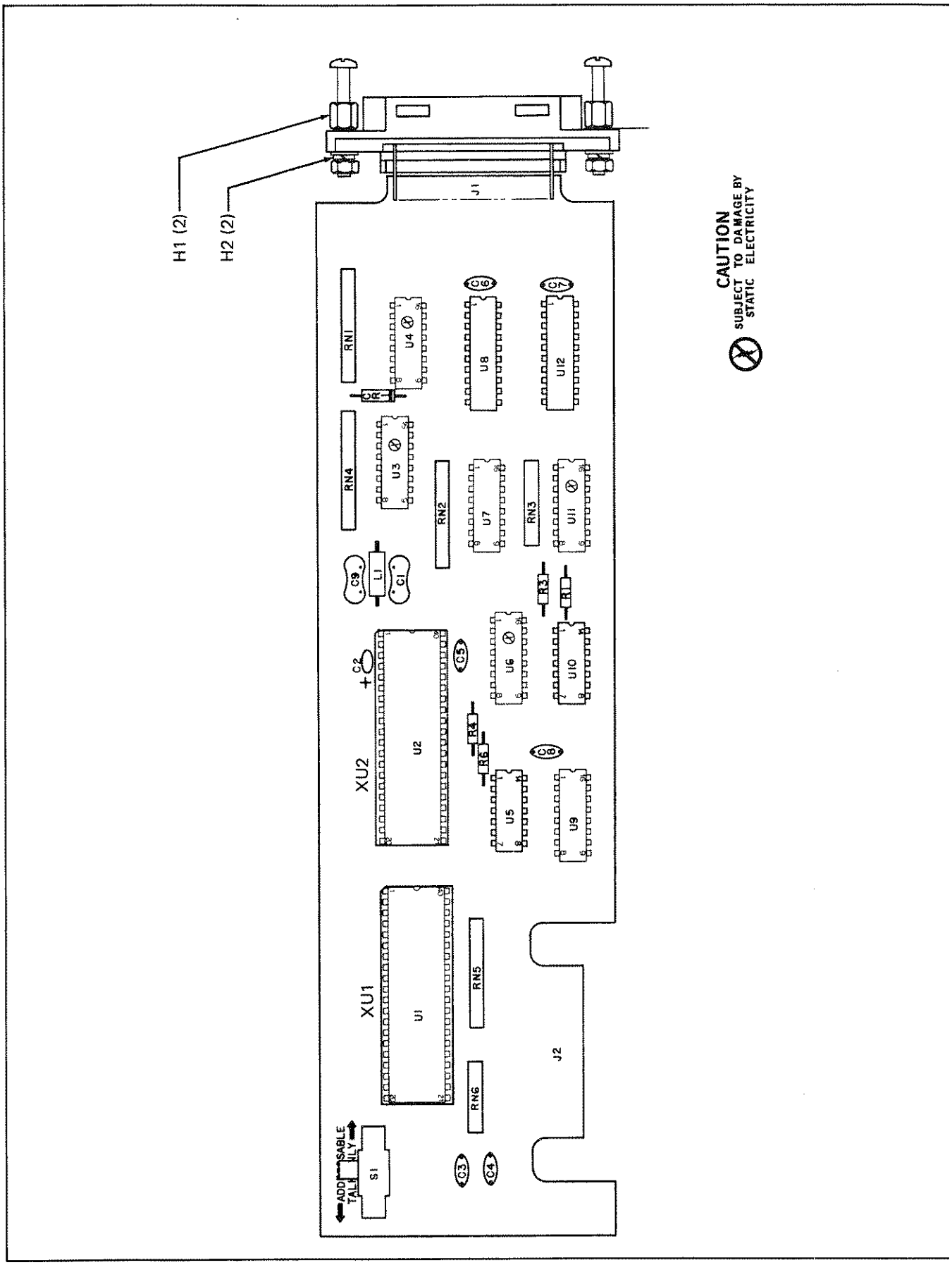


Figure 6522-5. Interface PCB Assembly

Option -529
IEEE Interface

6529-1. INTRODUCTION

6529-2. The IEEE Interface (Option -529) fulfills the particular requirements for interfacing a counter (7220A, 7250A, 7260A or 7261A) to the IEEE-488 bus. This option supplies the user with components necessary for interfacing. These items include a Data I/O Unit (Option -521) for installation in the counter, an Interface PCB Assembly (Option -522) to be installed in the 1120A IEEE-488 Translator, and an interconnecting cable (Y7203). Full programming and data sampling are available when this option is used with the 7260A or 7261A. Output only capabilities are available with the 7250A or 7220A. Programming commands are listed by applicable counter in Table 6529-1.

Table 6529-1. Programming Commands

CODE	DESCRIPTION		USED WITH			
			7220A	7250A	7260A	7261A
F0	FREQ A	FUNCTION COMMANDS			X	X
F1	Ratio A/B				X	X
F2	Period A				X	X
F3	Period Average A				X	X
F4	Time Interval				X	X
F5	Time Interval Average				X	X
F6	Frequency C				X	X
F7	Self Check				X	X
F8	Counts Per Minute				X	X
F9	Totalize (with the 7250A, F9 must be sent for remote operations if instrument has been manually set to TOT A)			X	X	X
R0	10^0 /100 μs	RESOLUTION COMMANDS			X	X
R1	10^1 /1 ms				X	X
R2	10^2 /10 ms				X	X
R3	10^3 /100 ms				X	X
R4	10^4 /1s				X	X
R5	10^5 /10s				X	X
R7	AUTO				X	X

Table 6529-1. Programming Commands (cont)

CODE	DESCRIPTION	USED WITH			
		7220A	7250A	7260A	7261A
C	Clears previous operating modes to the preset condition (M0, H0, J0)	X	X		
	Clears to M0, H0, J0, F0, R0, A+, B+, D0)			X	X
E	Reset instrument (display will clear and instrument begins a new reading if not in HOLD).	X	X	X	X
G	Get Status. For each "G" command, status is gathered once from the instrument and placed in an output buffer. Status is output the next time a reading is requested over the bus.	X	X	X	X
H0	Continuous trigger mode in which the instrument automatically cycles through the measurement routine.	X	X	X	X
H1	Hold mode, in which a new reading is initiated by the instrument only after a trigger command is received via the IEEE-488 interface.	X	X	X	X
J0	No line feeed suppression on output.	X	X	X	X
J1	Line feed suppression on output.	X	X	X	X
M0	No Service Request	X	X	X	X
M1	SRQ is sent after the instrument reading has been gathered.	X	X	X	X
T	Trigger. Sets Interface Trigger state and End of Message state true.	X	X	X	X
X	Retransmit. Sets RTRNS state in Interface true.	X	X	X	X
A+	Set slope for Channel A.			X	X
A−				X	X
B+	Set slope for Channel B.			X	X
B−				X	X
D0	Disengage 100 kHz filter.			X	X
D1	Engage 100 kHz filter.			X	X

6529-3. INSTALLATION

6529-4. Installation of the Data I/O Unit in the counter is detailed in subsection 6521 of this manual. Instructions for installing the Interface PCB Assembly are covered in subsection 6522. Refer to Figure 6529-1 for an overview of IEEE interfacing connections.

6529-5. THEORY OF OPERATION

6529-6. Operating theory for the IEEE Interface is presented separately for Option -521 and -522. The 1120A Instruction Manual explains IEEE-488 bus operation. Schematic diagrams for the Data I/O Unit and the Interface PCB Assembly are included in Section 8 of this manual. Figure 6529-2 provides a timing diagram of a data response from the counter.

6529-7. IEEE INTERFACE PERFORMANCE TESTING AND TROUBLESHOOTING

6529-8. Refer to Table 6529-2 for an overall list of equipment needed for this testing and troubleshooting procedure.

6529-9. Equipment Preparation (1120A)

6529-10. Complete the following procedure for preparation of the 1120A IEEE-488 Translator:

1. Ensure that only device 0 position (IF0) is occupied with an Interface PCB Assembly.

2. Place front panel address switches A3, A4 and A5 in the down (0) position.

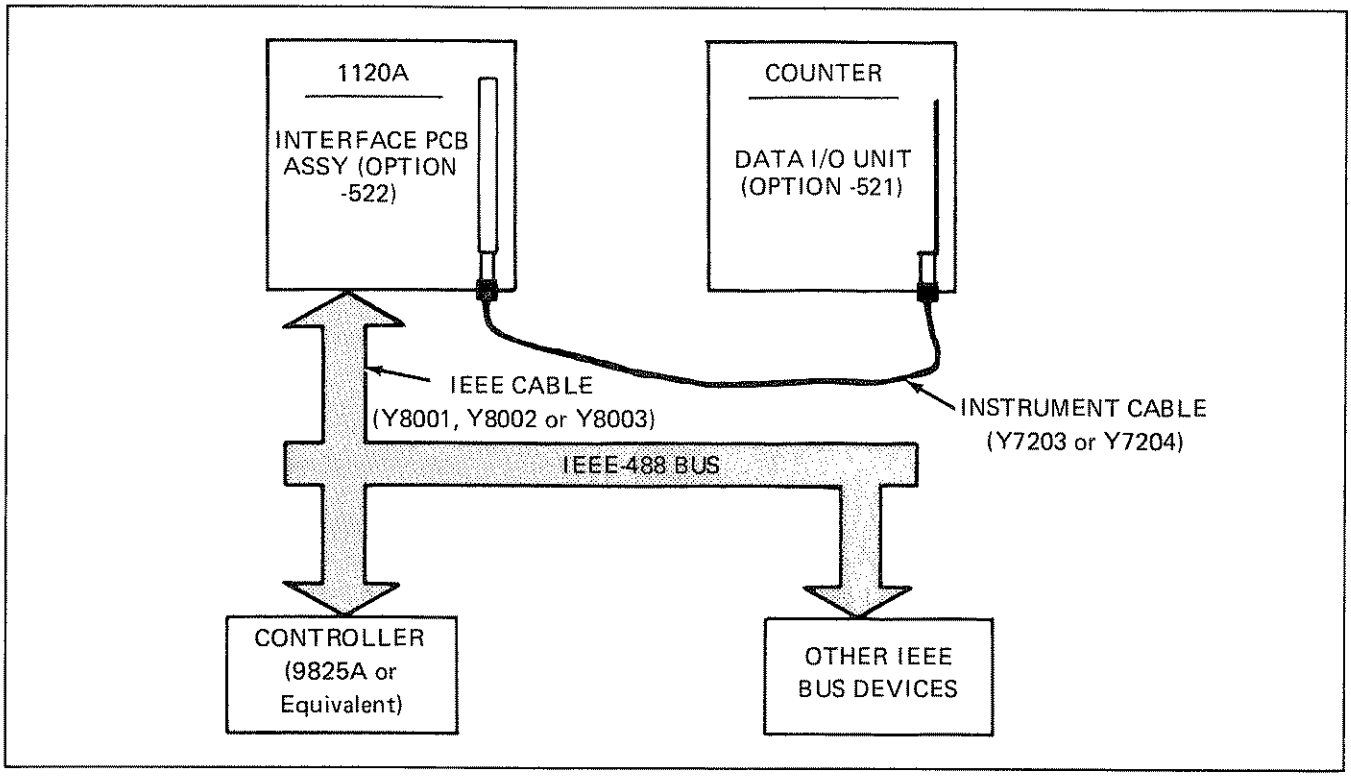
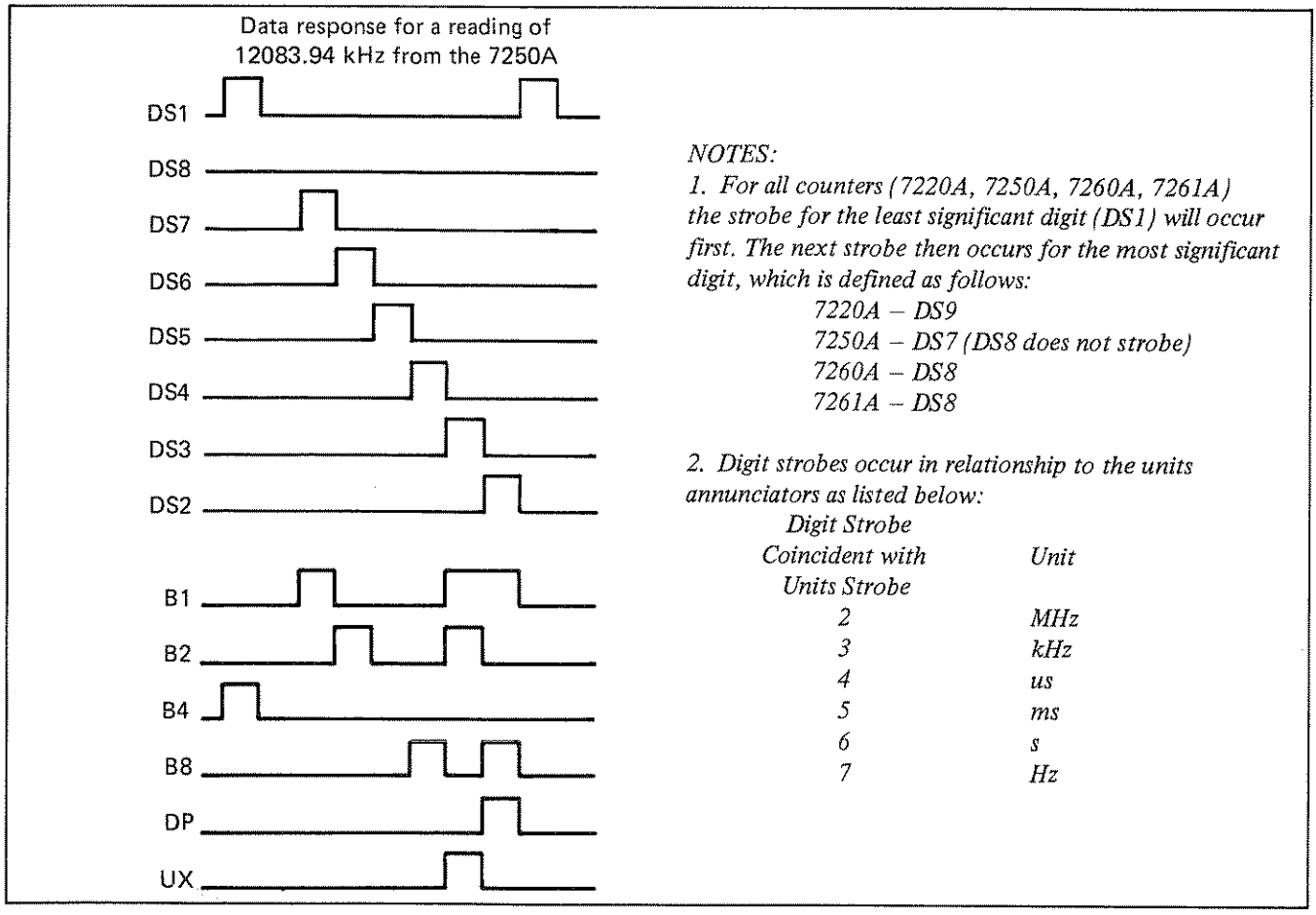


Figure 6529-1. Instrument Connections



NOTES:

1. For all counters (7220A, 7250A, 7260A, 7261A) the strobe for the least significant digit (DS1) will occur first. The next strobe then occurs for the most significant digit, which is defined as follows:

7220A – DS9
7250A – DS7 (DS8 does not strobe)
7260A – DS8
7261A – DS8

2. Digit strobes occur in relationship to the units annunciators as listed below:

Digit Strobe Coincident with Units Strobe	*Unit*
2	*MHz*
3	*kHz*
4	*us*
5	*ms*
6	*s*
7	*Hz*

Figure 6529-2. Timing Diagram

3. Verify that the TALK ONLY switch on the Interface PCB Assembly is in the "addressable" position.

4. Reinstall the 1120A's top cover.

5. Connect an instrument cable (Y7203 or Y7204) to the Interface PCB Assembly connector.

Table 6529-2. Performance Testing and Troubleshooting Required Equipment

IEEE BUS INTERFACING EQUIPMENT
1. Counter (7220A, 7250A, 7260A or 7261A)
2. Data I/O Unit with instrument cable (Option -521K) for counter
3. 1120A IEEE-488 Translator
4. Interface PCB Assembly (Option -522K)
5. IEEE Cable (Y8001, Y8002 or Y8003)
6. IEEE Bus Controller (HP9825A or equivalent)
TEST EQUIPMENT
1. Digital Multimeter
2. Oscilloscope (dual trace)
3. Bus Analyzer

6529-11. Equipment Preparation (Counter)

6529-12. Complete the following steps when connecting the counter in the IEEE interfacing system:

1. Ensure that the Data I/O Unit (Option -521) is properly installed in the counter. Refer to INSTALLATION included with Option -521 information.

2. If applicable, ensure that the counter's rear panel trigger mode switch is set to CONT (continuous).

3. Ensure that the counter's rear panel time base select switch is set to INT.

4. Connect the other end of the instrument cable to the Data I/O Unit connector.

6529-13. Equipment Preparation (IEEE Bus)

6529-14. Connect the 1120A to a controlling instrument with an IEEE cable (Y8001, Y8002 or Y8003). Ensure that all other IEEE devices and cables are disconnected. Examples given in this test and troubleshooting routine apply to the HP 9825A Calculator.

6529-15. Test Procedure

6529-16. An overall systems test procedure is presented in Table 6529-3. This procedure specifies test points on the Interface PCB Assembly (Option -522). Generally, signed conditions at these test points can be used as a first step in troubleshooting the 1120A mainframe, the IEEE bus connection, the instrument cable or the Data I/O Unit (Option -521) installed in the counter.

6529-17. The test procedure consists of a tabular flow chart. When a step on this chart is completed, check for a decision transfer. If no decision is required, perform the next step in sequence.

6529-18. REPLACEABLE PARTS

6529-19. Use the following information when ordering parts for the IEEE Interface Option:

PART	NUMBER
Data I/O Unit	72XXA-521
Interface PCB Assembly	72XXA-522
Instrument Cable (2 ft.)	Y7203
Instrument Cable (5 ft.)	Y7204

A further parts breakdown is presented with Options -521 and -522.

Table 6529-3. IEEE Interface Testing and Troubleshooting

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
	NOTE *All component designations apply to the Interface PCB Assembly unless otherwise noted.*		
1	Program the controller to address the counter with the assigned Listen address (address 0).		
2	Does the 1120A Device 0 Listen indicator illuminate?	23	3
3	Check U1-6 for a clock waveform of approximately 150 kHz with rise and fall times less than 50 ns.	8	4
4	Check for 150 kHz at U2-11.	6	5
5	Check for foreign matter or improper connections near pins 2 and 3 of U2, or near C1, L1 and C9. Repair as required and return to step 1.		7
6	Replace U5 and return to step 1.		
7	Replace U2 and resume at step 1.		
8	Connect a bus exerciser to the IEEE bus. This device should be capable of independently asserting an active low and a passive high on any or all of the interface bus lines. *NOTE* *It may be necessary to disconnect the controller from the bus during the tests involving a bus exerciser.*		
9	On the bus exerciser, assert DAV true (low), NDAC false (high) and NRFD false (high). Test for NDAC false and NRFD true.	10	11
10	Assert DAV false (high) and test for NDAC true and NRFD false.	23	11
11	Check for proper handshake operation.	16	12
12	Using the bus exerciser, toggle the DAV line and check for DAV state change at U1-16.		
13	Verify that the following signal lines toggle in a similar manner: NDAC U1-17 NRFD U1-18 IFC U1-21 REN U1-22 SRQ U1-23 EOI U1-25 ATN U1-26 DIO8 - DIO1 U1-29 through 36 respectively		
14	For any signals not toggling, check the Interface PCB and the 1120A Main PCB for broken or shorted connections. Repair as required and resume at step 9.		15

Table 6529-3. IEEE Interface Testing and Troubleshooting (cont)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
15	Cause a manual reset by grounding U1-19. Repeat steps 1, 10 and 11.	23	16
16	Check for a high at U2-36.	17	
17	Repair LED driver circuit and repeat step 1.	23	18
18	Check for negative going logic pulses at U1-37, 38, 39, 5 and 3.	20	19
19	Replace U2 and repeat step 1.	23	20
20	Toggle front panel 1120A control A3 and observe logic changes at U2-29.		
21	Check for toggling of A4 and A5 at U2-30 and U2-31. If necessary, repair and repeat step 1.	23	22
22	Replace U1 and resume at step 1.		
23	Send a "T" command from the controlling device (example: wrt 700, "T"). The counter should now be in remote mode, as evidenced by a faster gating rate than in local mode. If necessary, interrupt power to the 1120A and check for a slower rate when power is reapplied (in local). Now send another "T" command and check for a faster rate.	33	24
24	Check for the following outputs: (L = ≤ 0.4V; H = ≥2.4V): U12-2 (L) (J1-5) — U8-2 (L) (J1-18) U12-5 (L) (J1-3) — U8-5 (L) (J1-16) U12-6 (L) (J1-7) — U8-6 (L) (J1-15) U12-15 (L) (J1-4) — U8-15 (H) (J1-8) U12-16 (L) (J1-2) — U8-16 (H) (J1-6) U12-19 (L) (J1-1) — U8-19 (H) (J1-35) U12-9 (positive pulses) (J1-25) — U8-1 (L) (J1-19) U12-1 (L) (J1-19) If any of these outputs is incorrect, remove the instrument cable and repeat the output check.		
25	If the U12 and U8 outputs are good when the instrument cable is disconnected, but bad when the cable is connected, trace the affected signals back through the instrument cable and the counter Data I/O Unit to P4 on the counter Main PCB. Repair as required and resume at step 23.		26
26	If U12 and U8 outputs are still bad when the instrument cable is disconnected, place the controller in a looping program that outputs a "T" command to the counter. Example (9825A): 0: wrt 700, "H1" 1: wrt 700, "T"; jmp 0		
27	Check U7-1 for negative going pulses.		30
28	Change the controller program to output "E" in a loop.		30

Table 6529-3. IEEE Interface Testing and Troubleshooting (cont)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
29	Check U7-2 for negative going pulses.		30
30	If there are no negative going pulses on U7, trace the signal back through U10 to U2. If no signal is present on U10-5 or U6-1, there is a possible problem associated with the internal data bus. Check the data bus for a constant one or zero condition. In normal operation, the data bus lines will exhibit both logic levels on each bus line. If a constant one or zero is found, remove integrated circuits on the internal data bus until the fault causing device is found. Replace as required and resume at step 23.		
31	If no signal is present on U2-10 or U2-8, replace U2 and resume at step 23.		
32	If no signal is present on U10-6, replace U10 and resume at step 23.		
33	On the 7250A or 7220A, manually place FUNCTION in self check. With the 7260A or 7261A, use the controller to send the command "CF7H1T". Example (9825A): wrt 700, "CF7H1T"		
34	The GATE indicator on the counter should stop flashing.		
35	Address the counter as a talker and take in one reading. Example (9825A): red 700, A ; dsp A On the 1120A, the TALK indicator for Device 0 should come on.		36
36	If the talk indicator will not light, check U2-37 for a logic high. A high suggests a faulty LED driver circuit; repair as required. Recheck controller talk address and setting of 1120A address switches.	35	37
37	Connect the bus analyzer to the present bus configuration. Reset the controller, and set the following bus conditions using the analyzer: $\overline{\text{NRFD}}$ - true (low) $\overline{\text{NDAC}}$ - true (low) $\overline{\text{DAV}}$ - false (high)		
38	Execute a trigger command from the controller, followed by a read command. Example (9825A): wrt 700, "T"; red 700, A; dsp A *NOTE* *The counter is now in the H1 mode; a trigger command must precede each read command to the counter interface. Otherwise, the interface will hang up on the read command.*		
39	The bus handshake is now under control of the bus analyzer. To handshake the first byte across the bus, set $\overline{\text{NRFD}}$ false, then true. At this point, the controller will be placing the first byte (UNLISTEN command) on the data bus lines. Examine the data lines to determine if the byte is correct as defined below: Data Bus — Command 0 0 1 1 1 1 1 1 — Unlisten		

Table 6529-3. IEEE Interface Testing and Troubleshooting (cont)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
40	For each of the following bytes, toggle $\overline{\text{NDAC}}$ false, then true, and $\overline{\text{NRFD}}$ false then true. Data Bus — Command 0 0 1 0 0 0 0 0 — 1120A Device 0 Listen 0 1 0 1 0 1 0 0 — T (ASCII) 0 0 0 0 1 1 0 1 — Carriage Return (ASCII) 0 0 0 0 1 0 1 0 — Line Feed (ASCII) 0 0 1 1 1 1 1 1 — Unlisten 0 1 0 0 0 0 0 0 — 1120A Device 0 Talk		
41	The next handshake sequence will consist of the counter reading data. Check U1-27 for a logic high, indicating that the interface is in a talk mode.	43	42
42	Recheck the data bus lines; if there is no problem here, replace U1 and resume at step 1.		
43	If U1-27 is high, but there is still no output, check U1-40 (the interrupt request signal). This signal should pulse low for each successive output byte from the counter interface. If U1-40 remains at a logic low, replace U2 and resume at step 1.		
44	If the counter interface does not source out data when made a talker, check the busy signal on U4-12. This signal should be low, indicating a not busy condition. An incorrect logic level here suggests a bad instrument cable connection or a bad Data I/O Unit in the counter. Repair as required.	46	45
45	If a negative going pulse is not generated on U1-40, replace U1 and resume at step 1.		
46	The Counter Data I/O Unit output, when displayed on the calculator, should read 10000000.00 (10 MHz).		47
47	Check the digit strobes at the following points: U3-2 (DS1), U3-4 (DS2), U3-6 (DS3), U3-10 (DS4), U11-14 (DS5), U11-12 (DS6), U14-2 (DS7), U14-4 (DS8), U14-6 (DS9) These strobe signals should be positive pulses occurring once for each display cycle, with the following exceptions: DS9 is low on the 7260A, 7261A and 7250A. DS8 is low on the 7250A. Figure 6529-2 and Table 6529-2 define strobe timing. If there are any strobe irregularities, trace the appropriate signal back through the instrument cable to the Data I/O Unit and P4 on the counter's Main PCB. Schematic diagrams, provided in Section 8 of this manual, may be used as an aid in signal tracing.		
48	If the decimal point or the order of magnitude of the reading appears incorrect, check U2-1 (decimal point) and U2-39 (units). With the counter programmed to F7 (or manually set to self check in the 7220A or 7250A), the units strobe should be coincident with DS2.		

Table 6529-3. IEEE Interface Testing and Troubleshooting (cont)

STEP NO.	ACTION	Go to the step number given for correct response	
		YES	NO
49	If there is no apparent problem with the digit strobes, check the data bits on U11 as follows: U11-2 - high (during one digit strobe) U11-4 - low U11-6 - low U11-10 - low		
50	Check status inputs to U4 and U3.		
51	Replace U4 and/or U3, as required.		
52	Check status at input to the Interface PCB Assembly;		
53	Check continuity of status signals through the instrument cable, the Data I/O Unit and the counter connector P4.		

Section 7
General Information

7-1. This section of the manual contains generalized user information as well as supplemental information to the List of Replaceable parts contained in Section 5. The following information is presented in this section:

List of Abbreviations
Federal Supply Codes for Manufacturers
Fluke Technical Service Centers — U.S. and Canada
Sales and Service Locations — International
Sales Representatives — U.S. and Canada

List of Abbreviations and Symbols

A or amp	ampere
ac	alternating current
af	audio frequency
a/d	analog-to-digital
assy	assembly
AWG	american wire gauge
B	bel
bcd	binary coded decimal
^{o}C	Celsius
cap	capacitor
ccw	counterclockwise
cer	ceramic
cermet	ceramic to metal(seal)
ckt	circuit
cm	centimeter
cmrr	common mode rejection ratio
comp	composition
cont	continue
crt	cathode-ray tube
cw	clockwise
d/a	digital-to-analog
dac	digital-to-analog converter
dB	decibel
dc	direct current
dmm	digital multimeter
dvm	digital voltmeter
elect	electrolytic
ext	external
F	farad
^{o}F	Fahrenheit
FET	Field-effect transistor
ff	flip-flop
freq	frequency
FSN	federal stock number
g	gram
G	giga (10^{9})
gd	guard
Ge	germanium
GHz	gigahertz
gmv	guaranteed minimum value
gnd	ground
H	henry
hd	heavy duty
hf	high frequency
Hz	hertz
IC	integrated circuit
if	intermediate frequency
in	inch(es)
intl	internal
I/O	input/output
k	kilo (10^{3})
kHz	kilohertz
kΩ	kilohm(s)
kV	kilovolt(s)
lf	low frequency
LED	light-emitting diode
LSB	least significant bit
LSD	least significant digit
M	mega (10^{6})
m	milli (10^{-3})
mA	milliampere(s)
max	maximum
mf	metal film
MHz	megahertz
min	minimum
mm	millimeter
ms	millisecond
MSB	most significant bit
MSD	most significant digit
MTBF	mean time between failures
MTTR	mean time to repair
mV	millivolt(s)
mv	multivibrator
MΩ	megohm(s)
n	nano (10^{-9})
na	not applicable
NC	normally closed
(–) or neg	negative
NO	normally open
ns	nanosecond
opnl ampl	operational amplifier
p	pico (10^{-12})
para	paragraph
pcb	printed circuit board
pF	picofarad
pn	part number
(+) or pos	positive
pot	potentiometer
p-p	peak-to-peak
ppm	parts per million
PROM	programmable read-only memory
psi	pound-force per square inch
RAM	random-access memory
rf	radio frequency
rms	root mean square
ROM	read-only memory
s or sec	second (time)
scope	oscilloscope
SH	shield
Si	silicon
serno	serial number
sr	shift register
Ta	tantalum
tb	terminal board
tc	temperature coefficient or temperature compensating
tcxo	temperature compensated crystal oscillator
tp	test point
u or μ	micro (10^{-6})
uhf	ultra high frequency
us or μs	microsecond(s) (10^{-6})
uut	unit under test
V	volt
v	voltage
var	variable
vco	voltage controlled oscillator
vhf	very high frequency
vlf	very low frequency
W	watt(s)
ww	wire wound
xfmr	transformer
xstr	transistor
xtal	crystal
xtlo	crystal oscillator
Ω	ohm(s)
μ	micro (10^{-6})

Federal Supply Codes for Manufacturers (Continued)

00213
Nytronics Comp. Group Inc.
Subsidiary of Nytronics Inc.
Formerly Sage Electronics
Rochester, New York

00327
Welwyn International, Inc.
Westlake, Ohio

00656
Aerovox Corp.
New Bedford, Massachusetts

00686
Film Capacitors, Inc.
Passaic, New Jersey

00779
AMP Inc.
Harrisberg, Pennsylvania

01121
Allen-Bradley Co.
Milwaukee, Wisconsin

01281
TRW Electronic Comp.
Semiconductor Operations
Lawndale, California

01295
Texas Instruments, Inc.
Semiconductor Group
Dallas, Texas

01537
Motorola Communications &
Electronics Inc.
Franklin Park, Illinois

01686
RCL Electronics Inc.
Manchester, New Hampshire

01730
Replaced by 73586

01884 - use 56289
Sprague Electric Co.
Dearborn Electronic Div.
Lockwood, Florida

02114
Ferroxcube Corp.
Saugerties, New York

02131
General Instrument Corp.
Harris ASW Div.
Westwood, Maine

02395
Rason Mfg. Co.
Brooklyn, New York

02533
Snelgrove, C.R. Co., Ltd.
Don Mills, Ontario, Canada
M3B 1M2

02606
Fenwal Labs
Div. of Travenal Labs.
Morton Grove, Illinois

02660
Bunker Ramo Corp., Conn Div.
Formerly Amphenol-Borg
Electric Corp.
Broadview, Illinois

02799
Areo Capacitors, Inc.
Chatsworth, California

03508
General Electric Co.
Semiconductor Products
Syracuse, New York

03614
Replaced by 71400

03651
Replaced by 44655

03797
Eldema Div.
Genisco Technology Corp.
Compton, California

03877
Transistron Electronic Corp.
Wakefield, Massachusetts

03888
KDI Pyrofilm Corp.
Whippany, New Jersey

03911
Clairex Electronics Div.
Clairex Corp.
Mt. Vernon, New York

03980
Muirhead Inc.
Mountainside, New Jersey

04009
Arrow Hart Inc.
Hartford, Connecticut

04062
Replaced by 72136

04202
Replaced by 81312

04217
Essex International Inc.
Wire & Cable Div.
Anaheim, California

04221
Aemco, Div. of
Midtex Inc.
Mankato, Minnesota

04222
AVX Ceramics Div.
AVX Corp.
Myrtle Beach, Florida

04423
Telonic Industries
Laguna Beach, California

04645
Replaced by 75376

04713
Motorola Inc. Semiconductor
Products
Phoenix, Arizona

04946
Standard Wire & Cable
Los Angeles, California

05082
Replaced by 94988

05236
Jonathan Mfg. Co.
Fullerton, California

05245
Components Corp. now
Corcom, Inc.
Chicago, Illinois

05277
Westinghouse Electric Corp.
Semiconductor Div.
Youngwood, Pennsylvania

05278
Replaced by 43543

05279
Southwest Machine &
Plastic Co.
Glendora, California

05397
Union Carbide Corp.
Materials Systems Div.
New York, New York

05571 - use 56289
Sprague Electric Co.
Pacific Div.
Los Angeles, California

05574
Viking Industries
Chatsworth, California

05704
Replaced by 16258

05820
Wakefield Engineering Inc.
Wakefield, Massachusetts

06001
General Electric Co.
Electronic Capacitor &
Battery Products Dept.
Columbia, South Carolina

06136
Replaced by 63743

06383
Panduit Corp.
Tinley Park, Illinois

06473
Bunker Ramo Corp.
Amphenol SAMS Div.
Chatsworth, California

06555
Beede Electrical Instrument Co.
Penacook, New Hampshire

06739
Electron Corp.
Littleton, Colorado

06743
Clevite Corp.
Cleveland, Ohio

06751
Components, Inc. Semcor Div.
Phoenix, Arizona

06860
Gould Automotive Div.
City of Industry, California

06961
Vernitron Corp., Piezo
Electric Div.
Formerly Clevite Corp., Piezo
Electric Div.
Bedford, Ohio

06980
Eimac Div.
Varian Associates
San Carlos, California

07047
Ross Milton, Co., The
South Hampton, Pennsylvania

07115
Replaced by 14674

07138
Westinghouse Electric Corp.,
Electronic Tube Division
Horsehead, New York

07233
TRW Electronic Components
Cinch Graphic
City of Industry, California

07256
Silicon Transistor Corp.
Div. of BBF Group Inc.
Chelmsford, MA

07261
Aumet Corp.
Culver City, California

07263
Fairchild Semiconductor
Div. of Fairchild Camera
& Instrument Corp.
Mountain View, California

07344
Bircher Co., Inc.
Rochester, New York

07597
Burndy Corp.
Tape/Cable Div.
Rochester, New York

07792
Lerma Engineering Corp.
Northampton, Massachusetts

07910
Teledyne Semiconductor
Formerly Continental Device
Hawthorne, California

07933 - use 49956
Raytheon Co.
Semiconductor Div. HQ
Mountain View, California

08225
Industro Transistor Corp.
Long Island City, New York

08261
Spectra Strip Corp.
Garden Grove, California

08530
Reliance Mica Corp.
Brooklyn, New York

08806
General Electric Co.
Miniature Lamp Products Dept.
Cleveland, Ohio

08863
Nytomatic Corp.
Norrisville, Pennsylvania

08988 - use 53085
Skottie Electronics Inc.
Archbald, Pennsylvania

09214
G.E. Co. Semi-Conductor
Products Dept.
Power Semi-Conductor
Products OPN Sec.
Auburn, New York

09353
C and K Components
Watertown, Massachusetts

09423
Scientific Components, Inc.
Santa Barbara, California

09922
Burndy Corp.
Norwalk, Connecticut

09969
Dale Electronics Inc.
Yankton, S. Dakota

10059
Barker Engineering Corp.
Formerly Amerace, Amerace
ESNA Corp.
Kenilworth, New Jersey

11236
CTS of Berne
Berne, Indiana

11237
CTS Keene Inc.
Paso Robles, California

11358
CBS Electronic Div.
Columbia Broadcasting System
Newburyport, MN

11403
Best Products Co.
Chicago, Illinois

11503
Keystone Columbia Inc.
Warren, Michigan

11532
Teledyne Relays
Hawthorne, California

11711
General Instrument Corp
Rectifier Division
Hickville, New York

11726
Qualidyne Corp.
Santa Clara, California

12014
Chicago Rivet & Machine Co.
Bellwood, Illinois

12040
National Semiconductor Corp.
Danburry, Connecticut

12060
Diodes, Inc.
Chatsworth, California

12136
Philadelphia Handle Co.
Camden, New Jersey

12300
Potter-Brumfield Division
AMF Canada LTD.
Guelph, Onatrio, Canada

12323
Presin Co., Inc.
Shelton, Connecticut

12327
Freeway Corp. formerly
Freeway Washer & Stamping Co.
Cleveland, Ohio

12443
Budd Co. The, Polychem Products
Plastic Products Div.
Bridgeport, PA

12615
U.S. Terminals Inc.
Cincinnati, Ohio

12617
Hamlin Inc.
Lake Mills, Wisconsin

12697
Clarostat Mfg. Co.
Dover, New Hampshire

12749
James Electronics
Chicago, Illinois

12856
Micrometals
Sierra Madre, California

12954
Dickson Electronics Corp.
Scottsdale, Arizona

12969
Unitrode Corp.
Watertown, Massachusetts

13103
Thermalloy Co., Inc.
Dallas, Texas

13327
Solitron Devices Inc.
Tappan, New York

13511
Amphenol Cadre Div.
Bunker-Ramo Corp.
Los Gatos, California

13606 - use 56289
Sprague Electric Co.
Transistor Div.
Concord, New Hampshire

13839
Replaced by 23732

14099
Semtech Corp.
Newbury Park, California

14140
Edison Electronic Div.
Mc Gray-Edison Co.
Manchester, New Hampshire

14193
Cal-R-Inc. formerly
California Resistor, Corp.
Santa Monica, California

14298
American Components, Inc.
an Insilco Co.
Conshohocken, Pennsylvania

14655
Cornell-Dublier Electronics
Division of Federal Pacific
Electric Co. Govt. Control Dept.
Newark, New Jersey

14752
Electro Cube Inc.
San Gabriel, California

14869
Replaced by 96853

14936
General Instrument Corp.
Semi Conductor Products Group
Hicksville, New York

15636
Elec-Trol Inc.
Saugus, California

15801
Fenwal Electronics Inc.
Div. of Kidde Walter and Co., Inc.
Framingham, Massachusetts

15818
Teledyne Semiconductors, formerly
Amelco Semiconductor
Mountain View, California

15849
Litton Systems Inc. Useco Div.
formerly Useco Inc.
Van Nuys, California

15898
International Business
Machines Corp.
Essex Junction, Vermont

15909
Replaced by 14140

16258
Space-Lok Inc.
Burbank, California

16299
Corning Glass
Electronic Components Div.
Raleigh, North Carolina

16332
Replaced by 28478

16473
Cambridge Scientific Ind.
Div. of Chemed Corporation
Cambridge, Maryland

16742
Paramount Plastics Fabricators, Inc.
Downey, California

16758
Delco Electronics
Div. of General Motors Corp.
Kokomo, Indiana

17001
Replaced by 71468

17069
Circuit Structures Lab.
Burbank, California

17338
High Pressure Eng. Co., Inc.
Oklahoma City, Oklahoma

17545
Atlantic Semiconductors, Inc.
Asbury Park, New Jersey

17856
Siliconix, Inc.
Santa Clara, California

17870
Replaced by 14140

18178
Vactec Inc.
Maryland Heights, Missouri

18324
Signetics Corp.
Sunnyvale, California

18612
Vishay Resistor Products Div.
Vishay Intertechnology Inc.
Malvern, Pennsylvania

18736
Voltronics Corp.
Hanover, New Jersey

18927
G T E Sylvania Inc.
Precision Material Group
Parts Division
Titusville, Pennsylvania

19451
Perine Machinery & Supply Co.
Seattle, Washington

19701
Electro-Midland Corp.
Mepco-Electra Inc.
Mineral Wells, Texas

20584
Enochs Mfg. Inc.
Indianapolis, Indiana

20891
Self-Organizing Systems, Inc.
Dallas, Texas

21604
Buckeye Stamping Co.
Columbus, Ohio

21845
Solitron Devices Inc.
Transistor Division
Riveria Beach, Florida

22767
ITT Semiconductors
Palo Alto, California

23050
Product Comp. Corp.
Mount Vernon, New York

23732
Tracor Inc.
Rockville, Maryland

23880
Stanford Applied Engrng.
Santa Clara, California

23936
Pamotor Div., Wm. J. Purdy Co.
Burlingame, California

24248
Replaced by 94222

24355
Analog Devices Inc.
Norwood, Massachusetts

24655
General Radio
Concord, Massachusetts

24759
Lenox-Fugle Electronics Inc.
South Plainfield, New Jersey

25088
Siemen Corp.
Isilen, New Jersey

25403
Amperex Electronic Corp.
Semiconductor &
Micro-Circuits Div.
Slatersville, Rhode Island

27014
National Semiconductor Corp.
Santa Clara, California

27264
Molex Products
Downers Grove, Illinois

28213
Minnesota Mining & Mfg. Co.
Consumer Products Div.
St. Paul, Minnesota

28425
Serv-/-Link formerly
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70485
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70563
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Geneva, Illinois

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Saint Louis, Missouri

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Chicago, Illinois

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Cinch Connector Operations Div.
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Driver, Wilber B., Co.
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Replaced by 06980

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Replaced by 90303

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General Instrument Corp.
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Alpha Wire Corp.
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Replaced by 49956

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97945
Penwalt Corp.
SS White Industrial Products Div.
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Replaced by 11358

98094
Replaced by 49956

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98388
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Replaced by 12749

98925
Replaced by 14433

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United States

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Zip: 95050
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COLORADO
Denver
Fluke Technical Center
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Orlando
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WASHINGTON
Mountlake Terrace
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Canada

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INDONESIA
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JAPAN
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1 Higashikata-machi
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John Fluke Mfg. Co., Inc.
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Tel. (206) 774-2211 Toll Free: (800) 426-0361 TWX: 910-449-2850 TLX: 32-0013 Cable: Fluke

United States

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940 N. Fern Creek Ave.
Orlando, FL 32803
(305) 896-4881

HI, Honolulu
EMC Corporation
2979 Ualena St.
Honolulu, HI 96819
(808) 847-1138

IL, Chicago
John Fluke Mfg. Co., Inc.
1400 Hicks Road
Rolling Meadows, IL 60008
(312) 398-0850

IN, Indianapolis
John Fluke Mfg. Co., Inc.
5610 Crawfordsville Rd.
Suite 802
Indianapolis, IN 46224
(317) 244-2456

MA, Waltham
John Fluke Mfg. Co., Inc.
244 Second Avenue
Waltham, MA 02154
(617) 890-1600

MD, Baltimore
John Fluke Mfg. Co., Inc.
11501 Huff Court
Kensington, MD 20795
(301) 881-3370
(301) 792-7060 (Baltimore)

MI, Detroit
John Fluke Mfg. Co., Inc.,
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Livonia, MI 48154
(313) 522-9140

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(612) 884-4336

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Kansas City, MO 64117
(816) 454-5836

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(314) 731-3388

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Greensboro, NC 27408
(919) 273-1918

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Clifton, NJ 07013
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Albuquerque, NM 87112
(505) 299-7658

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4515 Culver Road
Rochester, NY 14622
(716) 266-1400

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4756 Fishburg Rd.
Dayton, OH 45424
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PA, Philadelphia
John Fluke Mfg. Co., Inc.
1010 West 8th Ave., Suite H
King of Prussia, PA 19406
(215) 265-4040

TX, Austin
John Fluke Mfg. Co., Inc.
111 W. Anderson Lane
Suite 213
Austin ,TX 78752
(512) 458-6279

TX, Dallas
John Fluke Mfg. Co., Inc.
14400 Midway Road
Dallas, TX 75240
(214) 233-9990

TX, Houston
John Fluke Mfg. Co., Inc.
1014 Wirt Road, Suite 270
Houston, TX 77055
(713) 683-7913
(512) 222-2726 (San Antonio)

UT, Salt Lake City
Barnhill Three, Inc.
54 West 2100 South
Suite 3
Salt Lake City, UT 84115
(801) 484-4496

WA, Seattle
John Fluke Mfg. Co., Inc.
691 Strander Blvd.
Seattle, WA 98168
(206) 575-3765

Canada

ALB, Calgary
Allan Crawford Assoc., Ltd.
2280 - 39th N.E.
Calgary, ALB T2E 6P7
(403) 276-9658

BC, North Vancouver
Allan Crawford Assoc., Ltd.
3795 William Street
Burnaby, BC Y5C 3H3
(604) 294-1326

NS, Halifax
Allan Crawford Assoc., Ltd.
Suite 201, Townsend Pl.
800 Windmill Road
Burnside Industrial Park
Dartmouth, NS B3B 1L1
(902) 469-7865

ONT, Ottawa
Allan Crawford Assoc., Ltd.
1299 Richmond Road
Ottawa, ONT K2B 7Y4
(613) 829-9651

ONT, Toronto
Allan Crawford Assoc., Ltd.
6503 Northam Drive
Mississauga, ONT L4V 1J5
(416) 678-1500

QUE, Montreal
Allan Crawford Assoc., Ltd.
1330 Marie Victorin Blvd. E.
Longueuil, QUE J4G 1A2
(514) 670-1212

For Canadian areas not listed, contact the office nearest you or Allan Crawford Assoc. Ltd., Mississauga (Toronto), Ontario.

For more information on Fluke products or Sales Offices you may dial (800) 426-0361 toll free in most of U.S. From Alaska, Hawaii, Washington, or Canada phone (206) 774-2481. From other countries phone (206) 774-2398.

Appendix 7A
Manual Change Information

INTRODUCTION

This appendix contains information necessary to backdate the manual to conform with earlier pcb configurations. To identify the configuration of the pcb's used in your instrument, refer to the revision letter (marked in ink) on the component side of each pcb assembly. Table 7A-1 defines the assembly revision levels documented in this manual.

NEWER INSTRUMENTS

As changes and improvements are made to the instrument, they are identified by incrementing the revision letter marked on the affected pcb assembly. These changes are documented on the supplemental change/errata sheet which, when applicable, is inserted at the front of the manual.

OLDER INSTRUMENTS

To backdate this manual to conform with earlier assembly revision levels, perform the changes indicated in Table 7A-1.

CHANGES

There are no backdating changes at this printing. All pcb assemblies are documented at their original revision level.

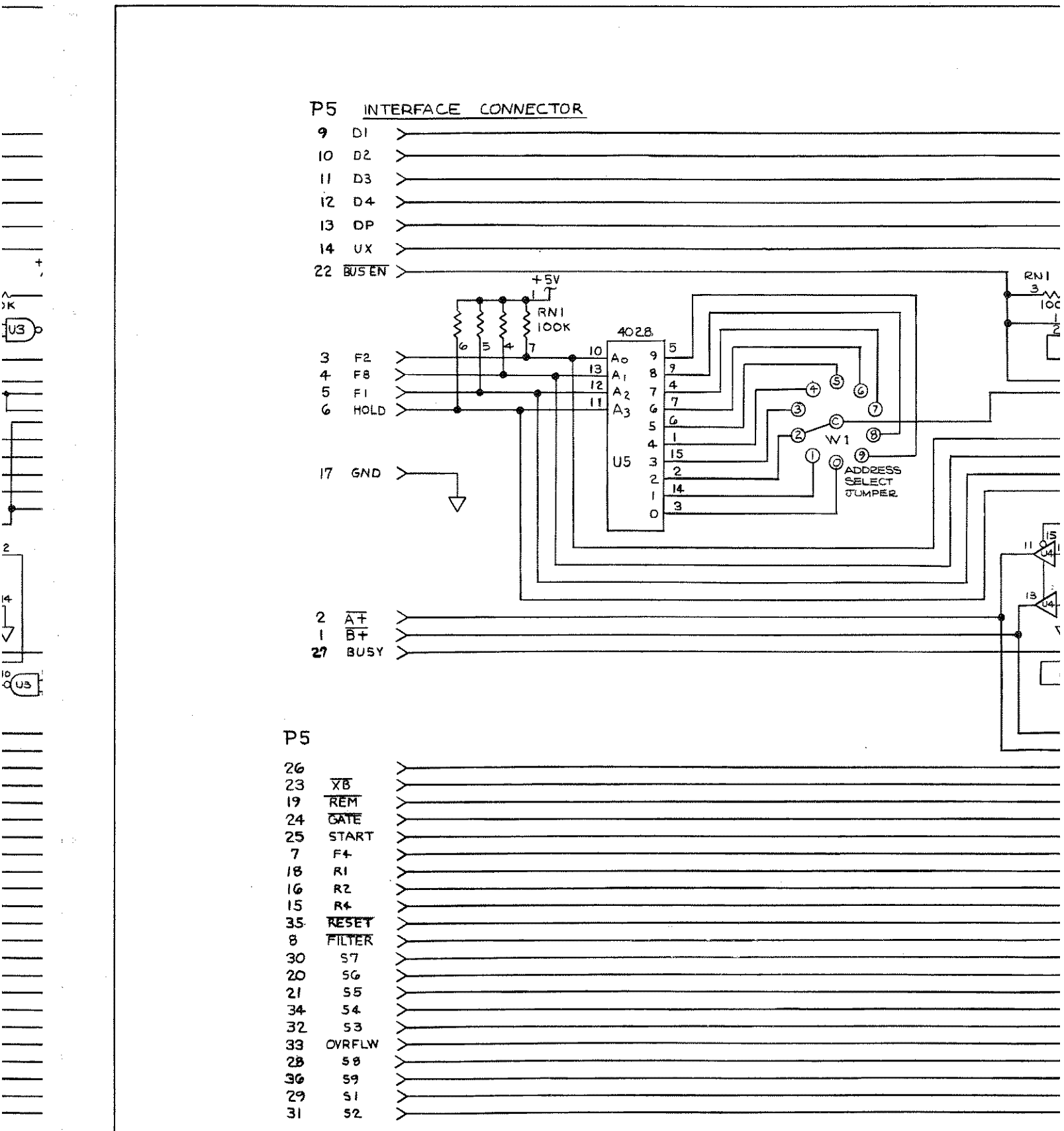
Table 7A-1. Manual Status and Backdating Information

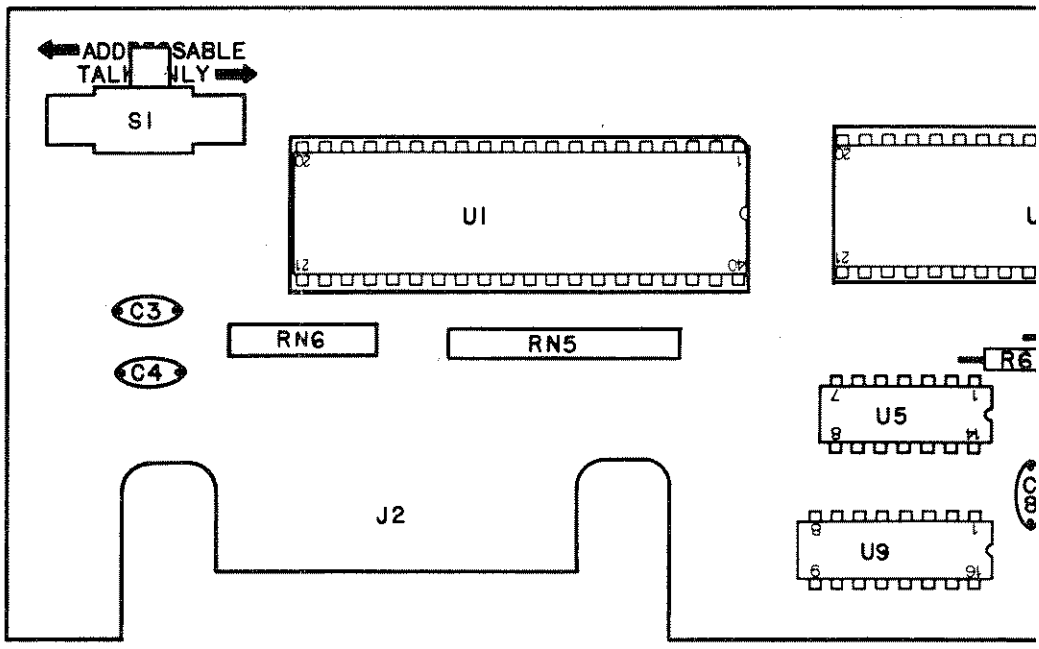
Ref Or Option No.	Assembly Name	Fluke Part No.	* To adapt manual to earlier rev configurations perform changes in desending order (by no.), ending with change under desired rev letter																				
			—	A	B	C	D	E	F	G	H	J	K	L	M	N	P							
A1	Main PCB Assembly	476689				X																		
A2	Front Panel PCB Assembly	476655			X																			
A3/A4	Signal Conditioner Assembly	479964								X														
A5	Free Air Time Base	406918			X																			
–010	Battery Option PCB Assembly	475962	X																					
–521	Data I/O Unit	487454			X																			
–522	Interface Pcb Assembly	476465				X																		

* X = The PCB revision levels documented in this manual.
● = These revision letters were never used in the instrument.
— = No revision letter on the PCB.

A0	Autorange feedback line to Control Logic (U13)
AR	Autorange feedback line to Control Logic (U13)
ASig	Signal line, Channel A, from fixed Attenuation control (X1, X10) to Signal Conditioner
BSig	Signal line, Channel B
BY	Busy signal from Control Logic (U13) when measurement sequence in progress
CI	1 MHz clock input to Control Logic (U13) 1/6 MHz in CPM mode
CO	TTL output from Control Logic (U13). High in CHK, PER AVG A; feeds 1 MHz through 10 Hz in TI A-B
CPM	Counts Per Minute
CR	Cycle rate
D1-D6	Digit one throughdigit six inputs to Control Logic for decimal point encoding
DP	Decimal Point
DS1-DS7	Display strobe lines
EA	TTL output from Control Logic: low in PER, PER AVG A, CHK
ECL Q ECL $\overline{Q}$	Complementary outputs from Signal Conditioner
EH	TTL output from Control Logic, Enables 10 MHz clock for TI A-B, PER A, CHK
F1L F2L F4L F8L	Local function control lines from front panel
F1R F2R F4R F8R	Remote function control lines from data output unit
F1 F2 F4 F8	Function control lines to Control Logic (U13) and CPM control
FILT	100 kHz filter control line
G	Gate annunciator enable
GC	Main Gate Flip-Flop clock
GQ	Main Gate enable
$\overline{GR}$	Main Gate Flip-Flop Reset
$\overline{GS}$	Main Gate Flip-Flop set
M1 M2 M3	Control Logic (U13) mode (function) inputs
$\overline{M}$	Memory update signal to Counter- Multiplexer (U15)
OVEN	Oven energized
OF	Overflow annunciator enable
QAECL	Complementary emitter coupled logic
$\overline{QAECL}$	inputs to Main PCB for Channel B
$\overline{R}$	Reset to display decade counters and overflow FF
R1 R2 R3	Control Logic inputs from RESOLUTION control
RI	Reset input to Control Logic (U13)
R1L R2L R4L	Range Rest Line from RESOLUTION control
SC	Single-Continuous Readings command to Control Logic
SLA+L	Positive slope command from front panel, Channel A
SLB+L	Positive slope command from front panel, Channel B
ST	Start command to Control Logic (U13)
TE	TTL output from Control Logic; high in TI A-B mode
TLA	Trigger offset control, Channel A
TLB	Trigger offset control, Channel B
TQ	TTL signal from Time Interval Flip-Flops, high at end of interval measurement
UX	Measurement units annunciation control
XA	TTL Channel A input signal to Control Logic or Time Interval Flip-Flops
XB	TTL Channel B input signal to Control Logic or Time Interval Flip-Flops

Figure 8-1. List of Mnemonics


P5 INTERFACE CONNECTOR
9 D1
10 D2
11 D3
12 D4
13 DP
14 UX
22 BUS EN
+5V
RN1
100K
4028
3 F2
4 F8
5 F1
6 HOLD
17 GND
U5
W1
ADDRESS SELECT JUMPER
2 A+
1 B+
27 BUSY
P5
26
23 XB
19 REM
24 GATE
25 START
7 F4
18 R1
16 R2
15 R4
35 RESET
8 FILTER
30 S7
20 S6
21 S5
34 S4
32 S3
33 OVRFLW
28 S0
36 S9
29 S1
31 S2


ADD SABLE
TALK NLY
S1
U1
C3
C4
RN6
RN5
R6
U5
J2
U9
C8